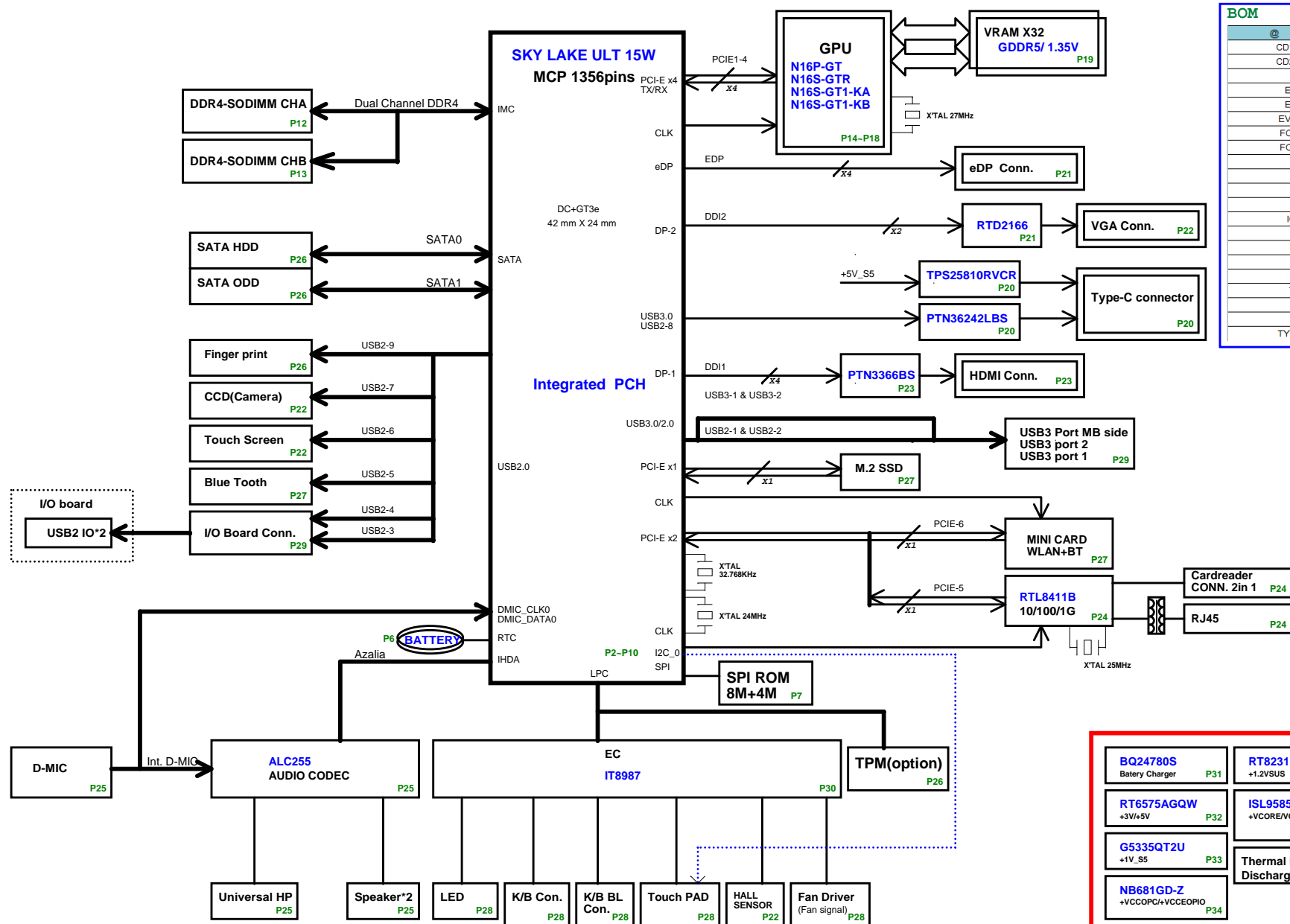


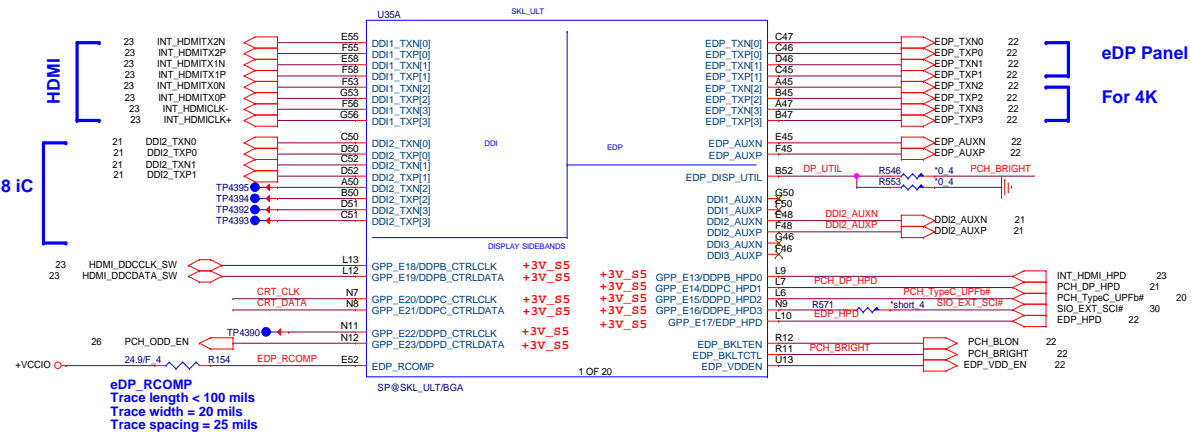
ZAAA Serials SkyLake-U SYSTEM BLOCK DIAGRAM



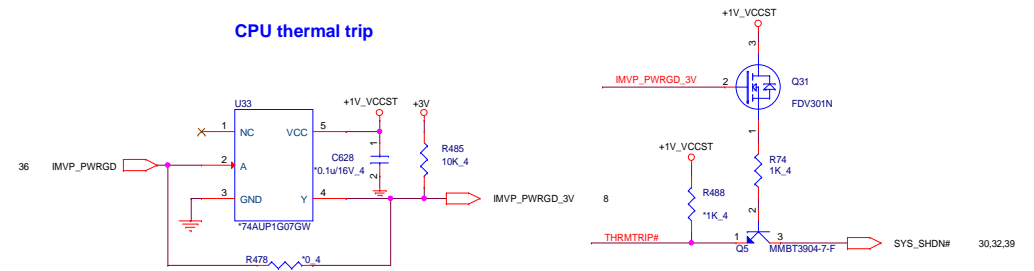
| CD | Function |
|---------|----------------------------------|
| CD1006@ | 22uF_0603 cost down to 10uF_0603 |
| CD2208@ | 47uF_0805 cost down to 22uF_0805 |
| EV @ | Discrete |
| EV_A@ | Discrete_940M_Kill B channel |
| EV_B@ | Discrete_940M_Kill A channel |
| EV_SP@ | Discrete_Spectral part |
| FOR15@ | For 15" |
| FOR17@ | For 17" |
| FPD@ | Finger Print |
| GC6@ | Discrete_GC6 |
| GS@ | G-sensor |
| GT3@ | UMA_GT3 |
| IOAC@ | with IOAC |
| IV@ | UMA |
| NAC@ | w/o IOAC |
| SP@ | Spectral Part |
| TDI@ | Touchpad INT |
| TPM@ | TPM |
| TSU@ | Touch Screen USB |
| TSI@ | Touch Screen i2C |
| TYPEC@ | Type-C function |

The diagram illustrates the power management architecture of the T1024 SoC. A central 'Thermal Protection Discharger' block is connected to several power regulators and components. The regulators include a 'Battery Charger' (BQ24780S) connected to a 3.1V regulator, a 'VGPU_CORE' regulator (UP1658RQKF) connected to a 3.6V regulator, and a 'VCCOPIA' regulator (NB681GD-Z) connected to a 3.4V regulator. Other regulators shown are RT6575AGQW (3.1V/5V), ISL9589HRTZ-T (VCORE/VCCSA/VCCGT), RT8068AZQW (1.05V_GFX), and G5335QT2U (1V_S5 and 1.35V_GFX).

SkyLake ULT (DISPLAY,eDP)

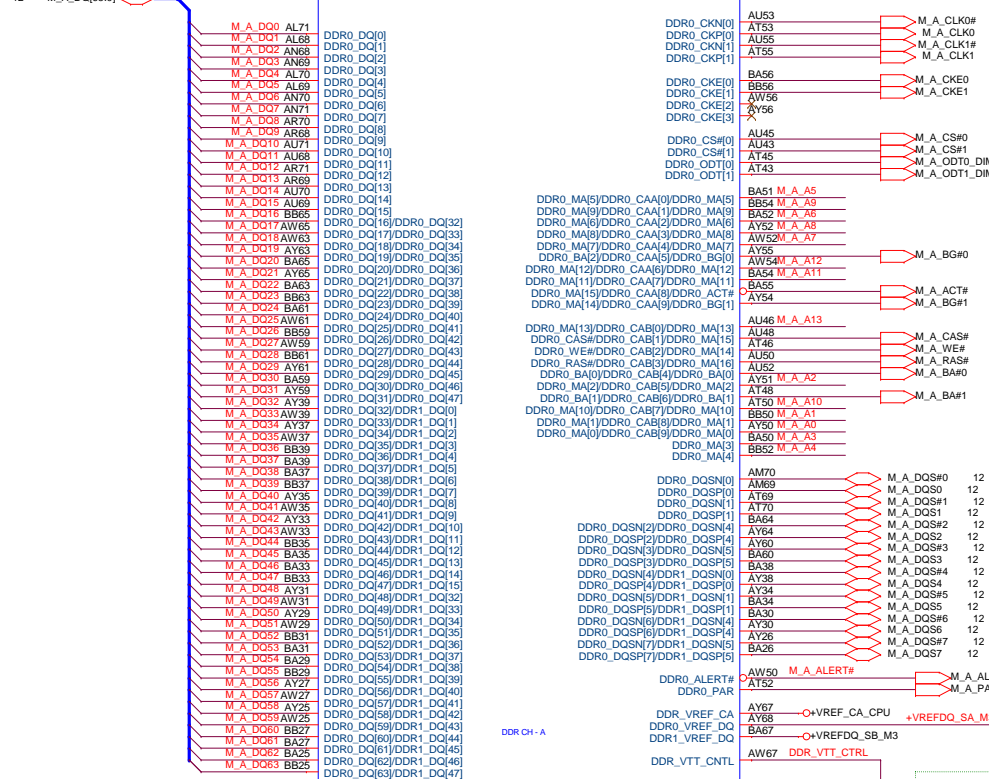


CPU thermal trip



| | | | | | | |
|--------------|-------------|-------------|-------------|--------------|-----------|-----------|
| M_A D00 AL71 | DDR0_DQ[0] | DDR0_CK[0] | DDR0_CK[0] | AU53 | M_A_CLK0 | M_A_CLK0# |
| M_A D01 AL68 | DDR0_DQ[1] | DDR0_CK[1] | DDR0_CK[1] | AU54 | M_A_CLK1 | M_A_CLK1# |
| M_A D02 AN68 | DDR0_DQ[2] | DDR0_CK[2] | DDR0_CK[2] | AU55 | M_A_CLK1# | M_A_CLK1 |
| M_A D03 AN69 | DDR0_DQ[3] | DDR0_CK[3] | DDR0_CK[3] | BA56 | M_A_CKE0 | M_A_CKE1 |
| M_A D04 AL70 | DDR0_DQ[4] | DDR0_CK[4] | DDR0_CK[4] | BB56 | M_A_CKE0 | M_A_CKE1 |
| M_A D05 AL69 | DDR0_DQ[5] | DDR0_CK[5] | DDR0_CK[5] | AW56 | M_A_CKE0 | M_A_CKE1 |
| M_A D06 AN70 | DDR0_DQ[6] | DDR0_CK[6] | DDR0_CK[6] | AY56 | M_A_CKE0 | M_A_CKE1 |
| M_A D07 AN71 | DDR0_DQ[7] | DDR0_CK[7] | DDR0_CK[7] | AA54 | M_A_CS#0 | M_A_CS#1 |
| M_A D08 AR70 | DDR0_DQ[8] | DDR0_CK[8] | DDR0_CK[8] | AA43 | M_A_CS#1 | M_A_CS#0 |
| M_A D09 AR68 | DDR0_DQ[9] | DDR0_CK[9] | DDR0_CK[9] | AT45 | M_A_ODT0 | M_A_ODT1 |
| M_A D10 AU71 | DDR0_DQ[10] | DDR0_CK[10] | DDR0_CK[10] | AT43 | M_A_ODT1 | M_A_ODT0 |
| M_A D11 AU68 | DDR0_DQ[11] | DDR0_CK[11] | DDR0_CK[11] | BA51 M_A_A5 | | |
| M_A D12 AR71 | DDR0_DQ[12] | DDR0_CK[12] | DDR0_CK[12] | BB54 M_A_A8 | | |
| M_A D13 AU70 | DDR0_DQ[13] | DDR0_CK[13] | DDR0_CK[13] | BB52 M_A_A9 | | |
| M_A D15 AU69 | DDR0_DQ[14] | DDR0_CK[14] | DDR0_CK[14] | AY54 M_A_A7 | | |
| M_A D16 BB65 | DDR0_DQ[15] | DDR0_CK[15] | DDR0_CK[15] | AY55 | | |
| M_A D17 AV65 | DDR0_DQ[16] | DDR0_CK[16] | DDR0_CK[16] | AW52 M_A_A7 | | |
| M_A D18 AW63 | DDR0_DQ[17] | DDR0_CK[17] | DDR0_CK[17] | AY56 | | |
| M_A D19 AY63 | DDR0_DQ[18] | DDR0_CK[18] | DDR0_CK[18] | AW54 M_A_A12 | | |
| M_A D20 BA65 | DDR0_DQ[19] | DDR0_CK[19] | DDR0_CK[19] | BA51 M_A_A11 | | |
| M_A D21 AY65 | DDR0_DQ[20] | DDR0_CK[20] | DDR0_CK[20] | BA55 | | |
| M_A D22 BA62 | DDR0_DQ[21] | DDR0_CK[21] | DDR0_CK[21] | AY54 | | |
| M_A D23 BB63 | DDR0_DQ[22] | DDR0_CK[22] | DDR0_CK[22] | AU46 M_A_A13 | | |
| M_A D24 BA61 | DDR0_DQ[23] | DDR0_CK[23] | DDR0_CK[23] | AU48 | | |
| M_A D25 AW61 | DDR0_DQ[24] | DDR0_CK[24] | DDR0_CK[24] | AT46 | | |
| M_A D26 BB59 | DDR0_DQ[25] | DDR0_CK[25] | DDR0_CK[25] | AA50 | | |
| M_A D27 AW59 | DDR0_DQ[26] | DDR0_CK[26] | DDR0_CK[26] | AU52 | | |
| M_A D28 BB61 | DDR0_DQ[27] | DDR0_CK[27] | DDR0_CK[27] | AY51 M_A_A2 | | |
| M_A D29 AY61 | DDR0_DQ[28] | DDR0_CK[28] | DDR0_CK[28] | AT50 M_A_A10 | | |
| M_A D30 BA59 | DDR0_DQ[29] | DDR0_CK[29] | DDR0_CK[29] | BB50 M_A_A1 | | |
| M_A D31 AY69 | DDR0_DQ[30] | DDR0_CK[30] | DDR0_CK[30] | AY50 M_A_A4 | | |
| M_A D32 AY39 | DDR0_DQ[31] | DDR0_CK[31] | DDR0_CK[31] | BA52 M_A_A9 | | |
| M_A D33 AW39 | DDR0_DQ[32] | DDR0_CK[32] | DDR0_CK[32] | AM70 | | |
| M_A D34 AY37 | DDR0_DQ[33] | DDR0_CK[33] | DDR0_CK[33] | AM69 | | |
| M_A D35 AW37 | DDR0_DQ[34] | DDR0_CK[34] | DDR0_CK[34] | AT69 | | |
| M_A D36 BB39 | DDR0_DQ[35] | DDR0_CK[35] | DDR0_CK[35] | AT70 | | |
| M_A D37 BA39 | DDR0_DQ[36] | DDR0_CK[36] | DDR0_CK[36] | AY64 | | |
| M_A D38 BA37 | DDR0_DQ[37] | DDR0_CK[37] | DDR0_CK[37] | AY64 | | |
| M_A D39 BB37 | DDR0_DQ[38] | DDR0_CK[38] | DDR0_CK[38] | AY60 | | |
| M_A D40 AY35 | DDR0_DQ[39] | DDR0_CK[39] | DDR0_CK[39] | BA60 | | |
| M_A D41 AW35 | DDR0_DQ[40] | DDR0_CK[40] | DDR0_CK[40] | BA38 | | |
| M_A D42 AY33 | DDR0_DQ[41] | DDR0_CK[41] | DDR0_CK[41] | AY38 | | |
| M_A D43 AW33 | DDR0_DQ[42] | DDR0_CK[42] | DDR0_CK[42] | AY34 | | |
| M_A D44 BB35 | DDR0_DQ[43] | DDR0_CK[43] | DDR0_CK[43] | BA30 | | |
| M_A D45 BA35 | DDR0_DQ[44] | DDR0_CK[44] | DDR0_CK[44] | AY30 | | |
| M_A D46 BA33 | DDR0_DQ[45] | DDR0_CK[45] | DDR0_CK[45] | AY26 | | |
| M_A D47 BB33 | DDR0_DQ[46] | DDR0_CK[46] | DDR0_CK[46] | BA26 | | |
| M_A D48 AY31 | DDR0_DQ[47] | DDR0_CK[47] | DDR0_CK[47] | | | |
| M_A D49 AW31 | DDR0_DQ[48] | DDR0_CK[48] | DDR0_CK[48] | | | |
| M_A D50 AY29 | DDR0_DQ[49] | DDR0_CK[49] | DDR0_CK[49] | | | |
| M_A D51 AW29 | DDR0_DQ[50] | DDR0_CK[50] | DDR0_CK[50] | | | |
| M_A D52 BB31 | DDR0_DQ[51] | DDR0_CK[51] | DDR0_CK[51] | | | |
| M_A D53 BA31 | DDR0_DQ[52] | DDR0_CK[52] | DDR0_CK[52] | | | |
| M_A D54 BA29 | DDR0_DQ[53] | DDR0_CK[53] | DDR0_CK[53] | | | |
| M_A D55 BB29 | DDR0_DQ[54] | DDR0_CK[54] | DDR0_CK[54] | | | |
| M_A D56 AY27 | DDR0_DQ[55] | DDR0_CK[55] | DDR0_CK[55] | | | |
| M_A D57 AW27 | DDR0_DQ[56] | DDR0_CK[56] | DDR0_CK[56] | | | |
| M_A D | | | | | | |

| | |
|-----|---------|
| 35B | SKL_ULT |
|-----|---------|



SP@SKL_ULT/BGA

M_A_A[13:0]

M_A_A[13:0] 12

R621 10K

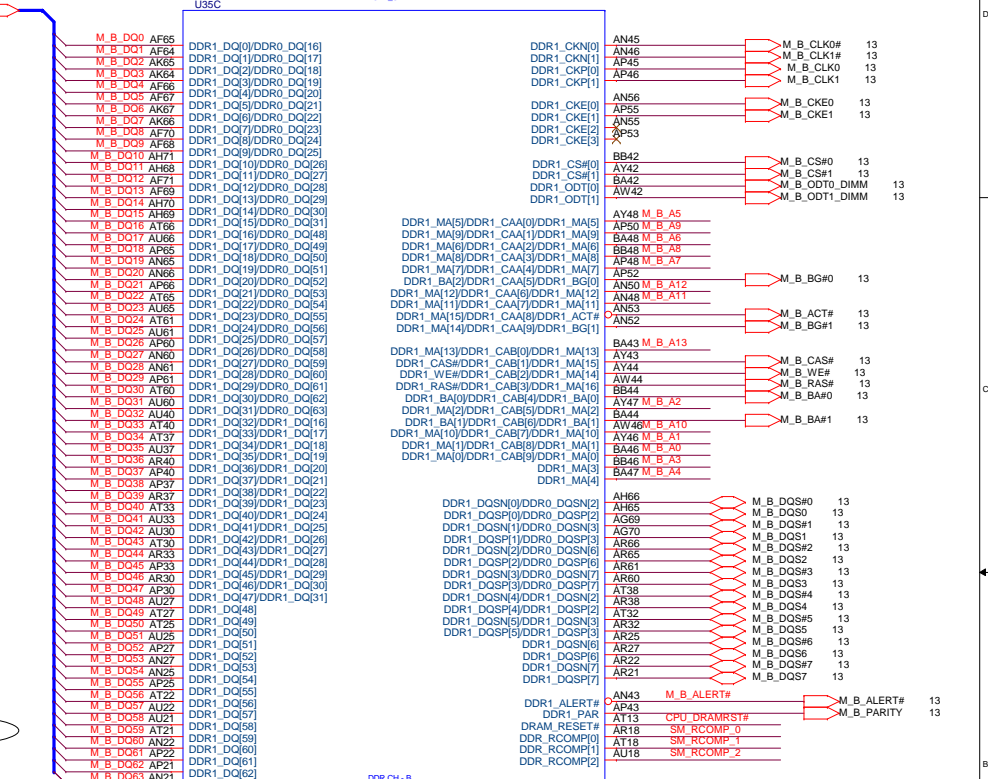
Q35 DTC144E

For Sx ,stuff Q? in

+3V_S5 2,4,6,7,8,9,11,20,24,26,27,28,30,32,34,35,40

CP

SKL_ULT



SP@SKL_ULI/BGA

M_B_A[13:0]

M_B_ALERT#

R11043

R11044

13

10 4

10 4

DRAM COMP

+1.2V_{SUS}

SM_RCOMP_0 121/F 4 R685

SM_RCOMP_1 80.6/F 4 R678

SM_RCOMP_2 100/F 4 R681

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470_4

| | | |
|---|------|--|
| 2 | DRAM | |
|---|------|--|

1

2 *0.1u/16V_4

| Size | Document Number | Rev |
|------|-----------------|-----|
|------|-----------------|-----|

Date: Monday, March 28, 2016 Sheet 3 of 48



PROJECT : ZAA

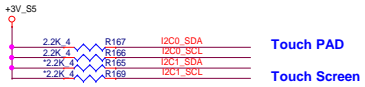
Skylake 2/3 (DDR3 I/F)

March 28, 2016 Sheet

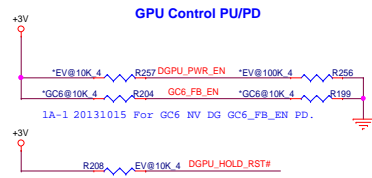
SKL ULT (SIDE BAND) GPIO

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

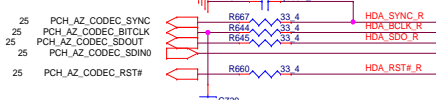


PU 2.2K for touch pad I2C bus(400 KHz)

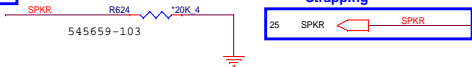


Touch PAD

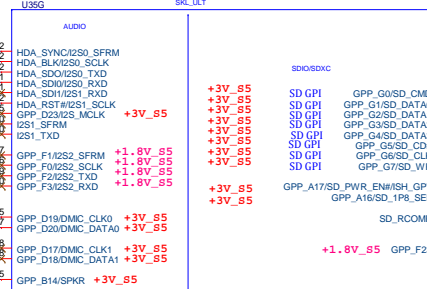
Touch Screen



| | DGPU_FW_CTRL# | VGA H/W Signal | Setup Menu | |
|-------------|---------------|-------------------|---------------|----------|
| UMA Only | 1 | UMA | Hidden | UMA boot |
| SG/Optimise | 0 | GPU | Hidden | GPU boot |









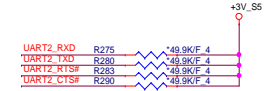
Strapping



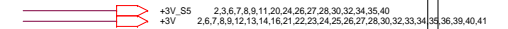
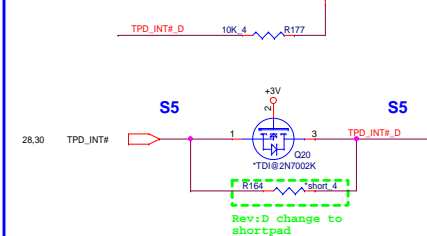
SP@SKL_ULT/BGA

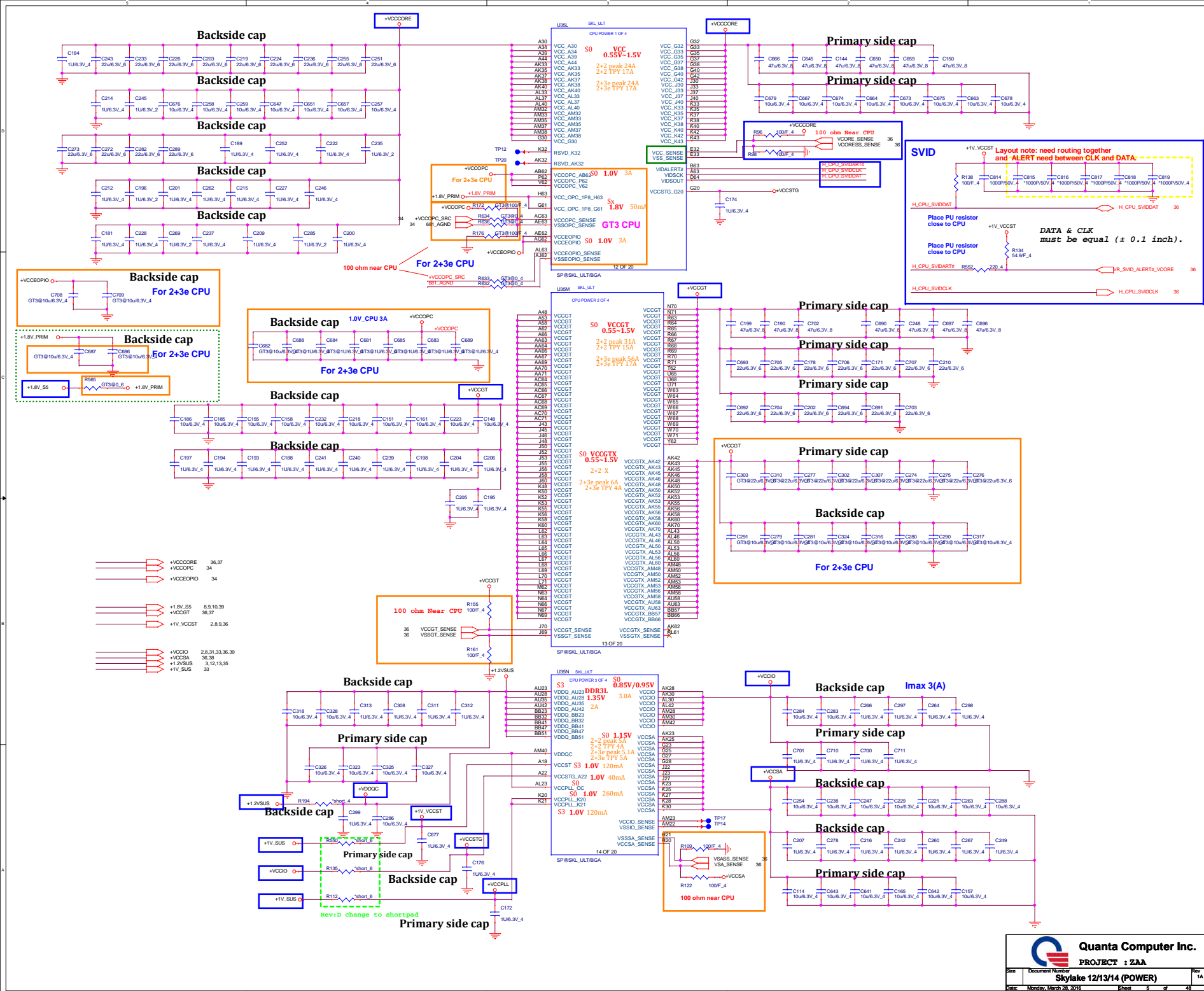
Skylake-U Strapping Table

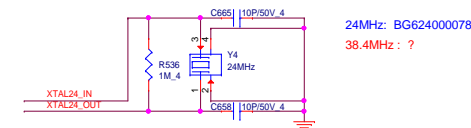
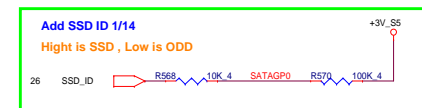
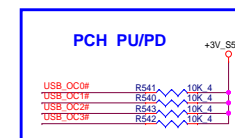
| Pin Name | Strap description | Sampled | Configuration | note |
|-------------------------------|--|-----------|---|--|
| GPP_B14 (SPKR) | Top-Block Swap override | PCH_PWROK | 0 = "Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode | +3V  SPKR |
| GPP_B18 (GSP10_MOSI) | No reboot | PCH_PWROK | 0 = "Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode | +3V  GSP10_MOSI |
| GPP_C2 (SMBALERT#) | TLS Confidentiality | RSMRST# | 0 = "Disable Intel ME Crypt to TLS(iPD 20K) 1 = Enable Intel ME Crypt to TLS | +3V_S5  SMBALERT# 7 |
| GPP_B22 (GSP11_MOSI) | Boot BIOS Strap Bit (BBS) | PCH_PWROK | 0 = "SPI (iPD 20K) 1 = LPC | +3V  GSP11_MOSI |
| GPP_C5 (SML0ALERT#) | eSPI or LPC | RSMRST# | 0 = "LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC | +3V_S5  SML0ALERT# 7 |
| SPI0_MOSI | Reserved | RSMRST# | (iPU 15 ~ 40K) | |
| SPI0_MISO | Reserved | RSMRST# | (iPU 15 ~ 40K) | |
| GPP_B23 (SML1ALERT# /PCHHOT#) | Reserved | RSMRST# | (iPD 20K) | |
| SPI0_IO2 | Reserved | RSMRST# | (iPU 15 ~ 40K) | |
| SPI0_IO3 | Reserved | RSMRST# | (iPU 15 ~ 40K) | |
| HDA_SDO / I2S_TXD0 | Flash Descriptor Security Override / Intel ME Debug Mode | PCH_PWROK | 0 = "Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override) | change location to near CPU to prevent impact HDA_SDO signal  ME_WR# 30 |
| GPP_E19 (DDPB_CTRLDATA) | Display Port B Detected | PCH_PWROK | 0 = "Port B is not detected (iPD 20K) 1 =Port B is detected | |
| GPP_E21 (DDPC_CTRLDATA) | Display Port C Detected | PCH_PWROK | 0 = "Port C is not detected (iPD 20K) 1 =Port C is detected | |



Touchpad INT



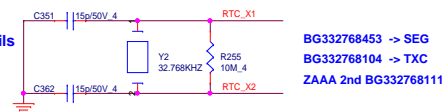




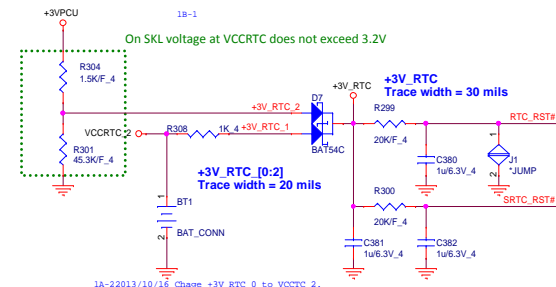
Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U



CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p



On SKL voltage at VCCRTC does not exceed 3.2V



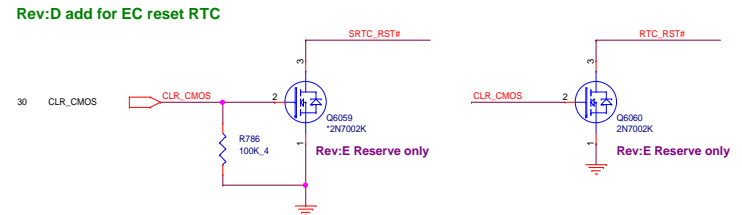
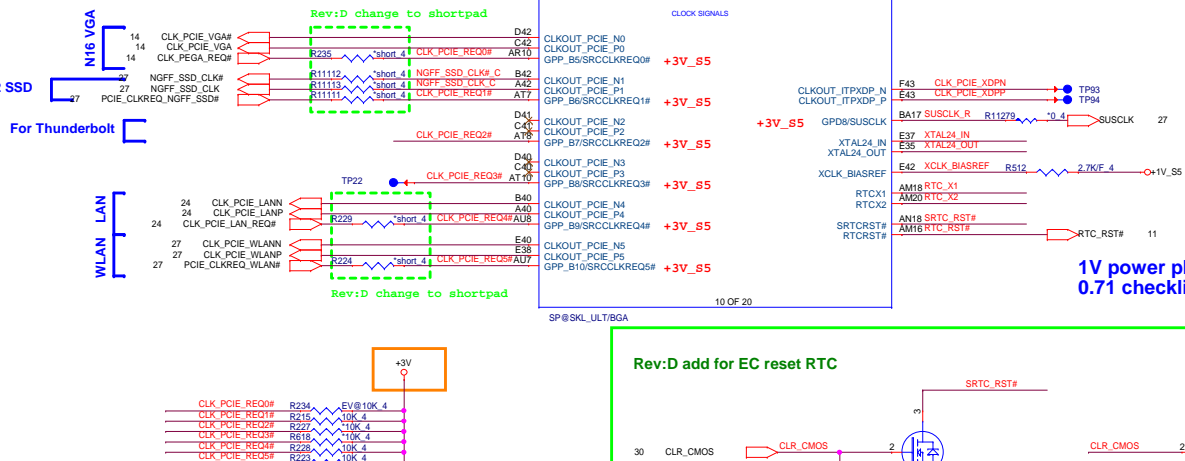
1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032



Quanta Computer Inc.

PROJECT : ZAA

| | | |
|-------|-----------------------------------|---------------|
| Size | Document Number | Rev |
| | Skylake 9/10 (PEG/USB/CLK) | 1A |
| Date: | Monday, March 28, 2016 | Sheet 6 of 48 |



1V power plane
0.71 checklist p14

Rev:D add for EC reset RTC

| | |
|-----------|--|
| SRIC_RST# | |
|-----------|--|

RTIC_F

| Age Group | Yes (%) | No (%) |
|-----------|---------|--------|
| 18-24 | ~75 | ~25 |
| 25-34 | ~65 | ~35 |
| 35-44 | ~55 | ~45 |
| 45-54 | ~45 | ~55 |
| 55-64 | ~35 | ~65 |
| 65+ | ~25 | ~75 |

CLER_CMOS

R786 2N7002R

2N7002K

1. *Journal of the American Medical Association*, 2000; 283: 2689-2693.

1

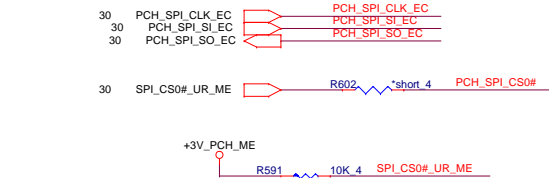
WWW.AliSaler.Com

For M.2 wifi module must



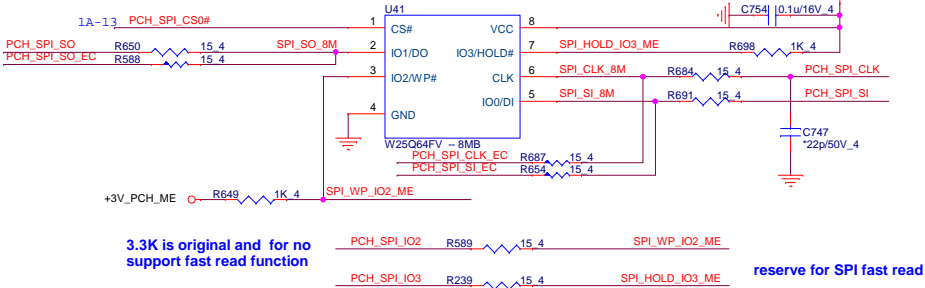
SP@ socket P/N: DFHS08FS023 only for A-TEST

| SPI ROM | Vender | Size | Quanta P/N | Vender P/N |
|--------------|--------|------|-------------|--------------|
| Skylake 3.3V | WND | 8M | AKE3EFP0N07 | W25Q64FVSSIQ |
| | GGD | 8M | AKE2EZN0Q00 | GD25B64CSIGR |
| | | | | |
| | | | | |
| | | | | |



PCH SPI ROM(8M+4M)

15ohm CS01502JB12
33ohm CS03302JB29

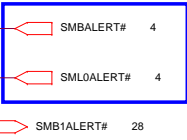


3.3K is original and for no support fast read function

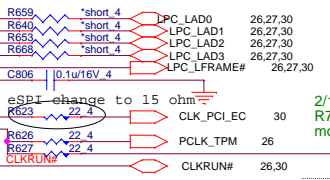
reserve for SPI fast read

+3V 2,4,6,8,9,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41
+3V_S5 2,3,4,6,8,9,11,20,24,26,27,28,30,32,34,35,40

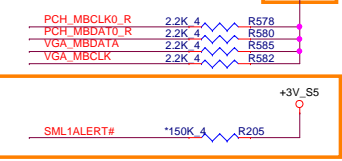
Strapping



eSPI change to 15 ohm ckl v0.71 p.24

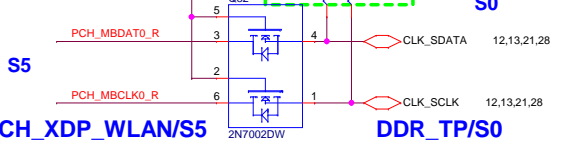


SMBus

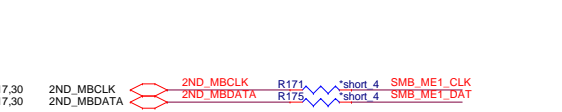


Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resistor

SMBus(PCH)



SMBus(EC)



EC/S5

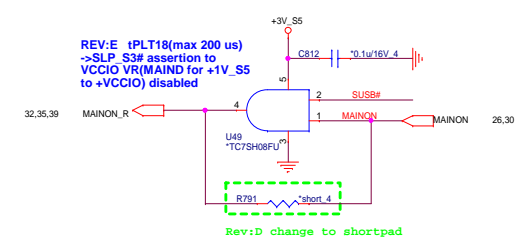
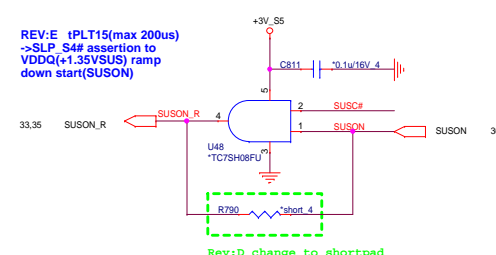
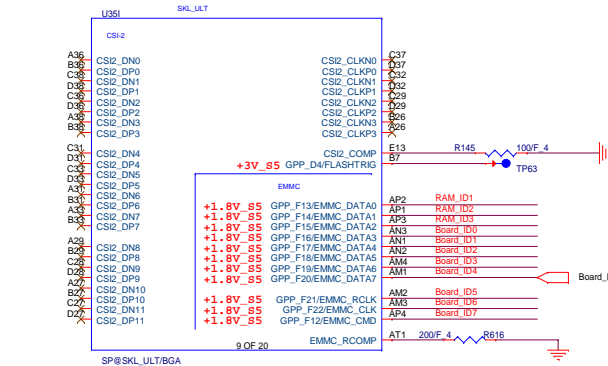
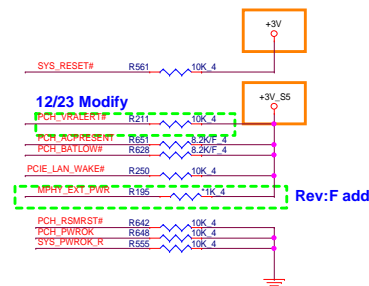


Quanta Computer Inc.

PROJECT : ZAA

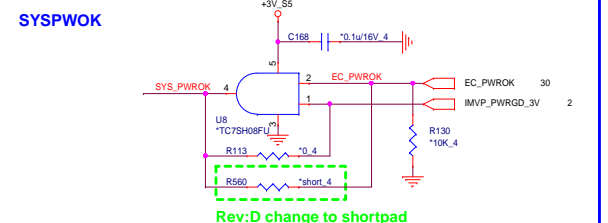
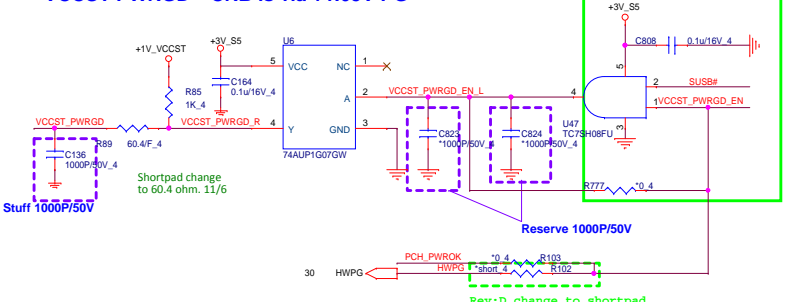
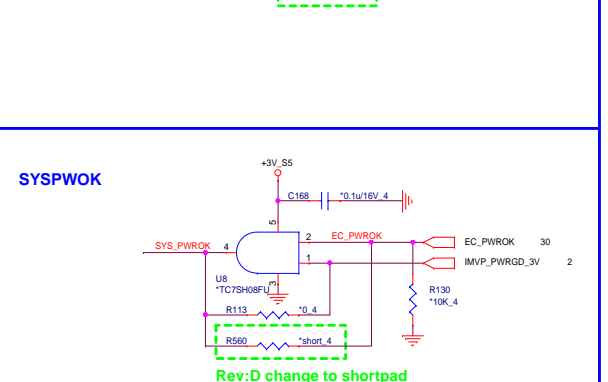
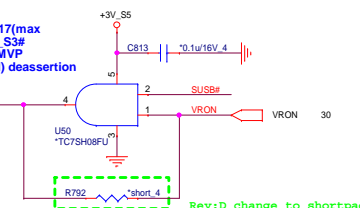
| Size | Document Number | Rev |
|------|--------------------------|-----|
| | Skylake 5 (SATA/HDA/SPI) | 1A |

Date: Monday, March 28, 2016 Sheet 7 of 48

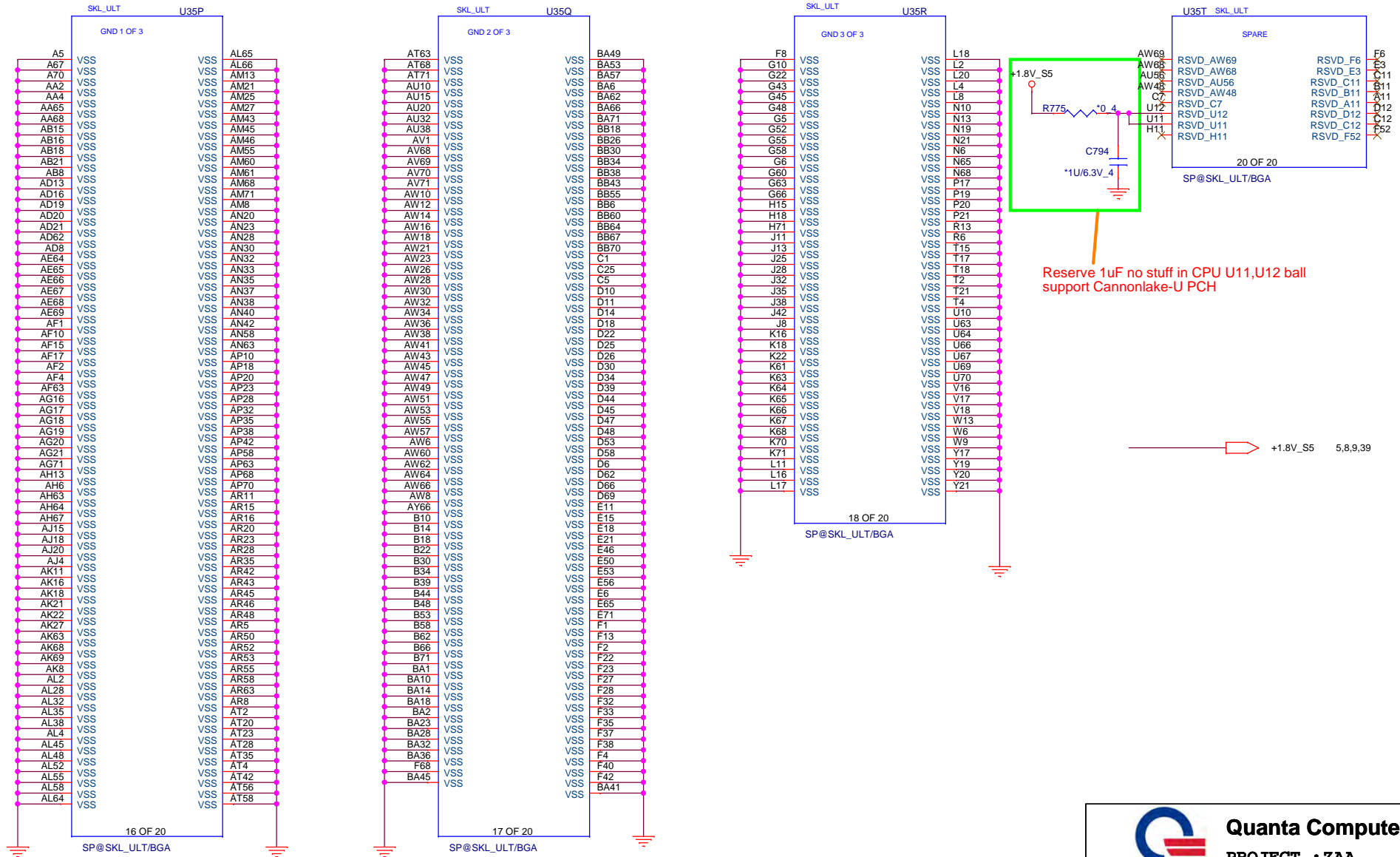



REV:E IPLT
200us) ->SLP
assertion to IIR
VR_ON(VRON

34,36 VRON_R 



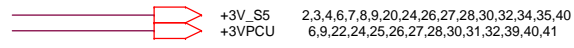
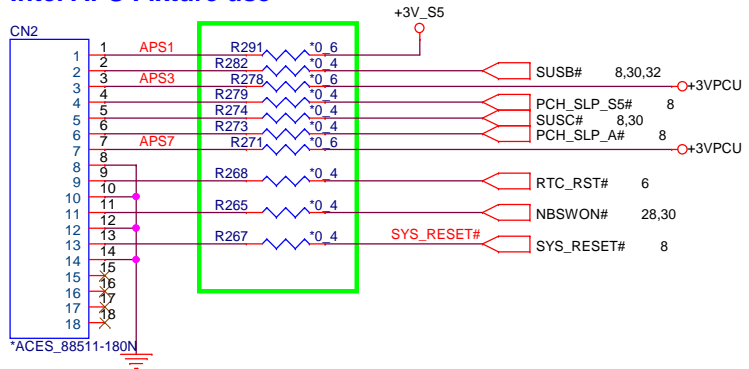
Skylake ULT (GND)

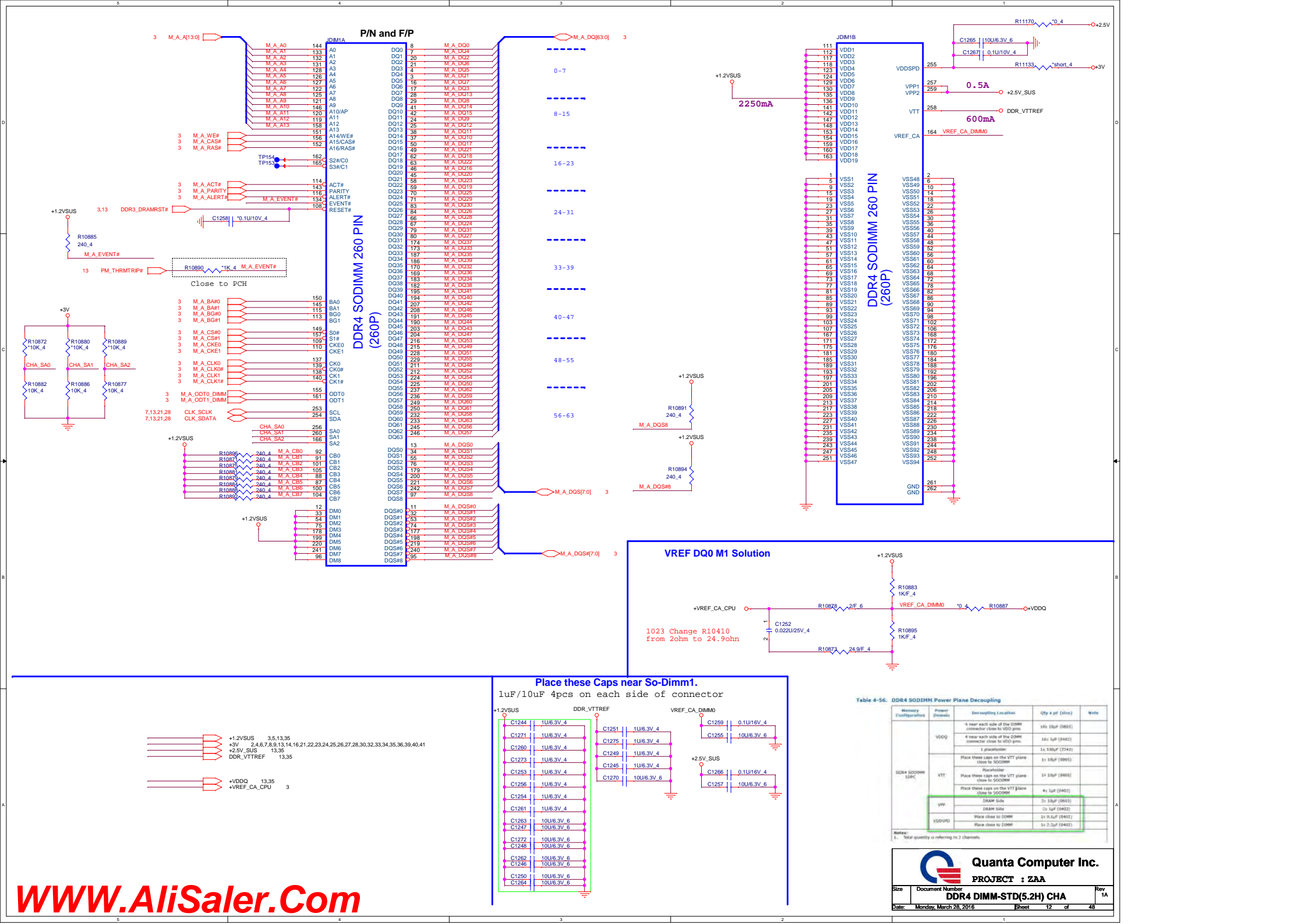


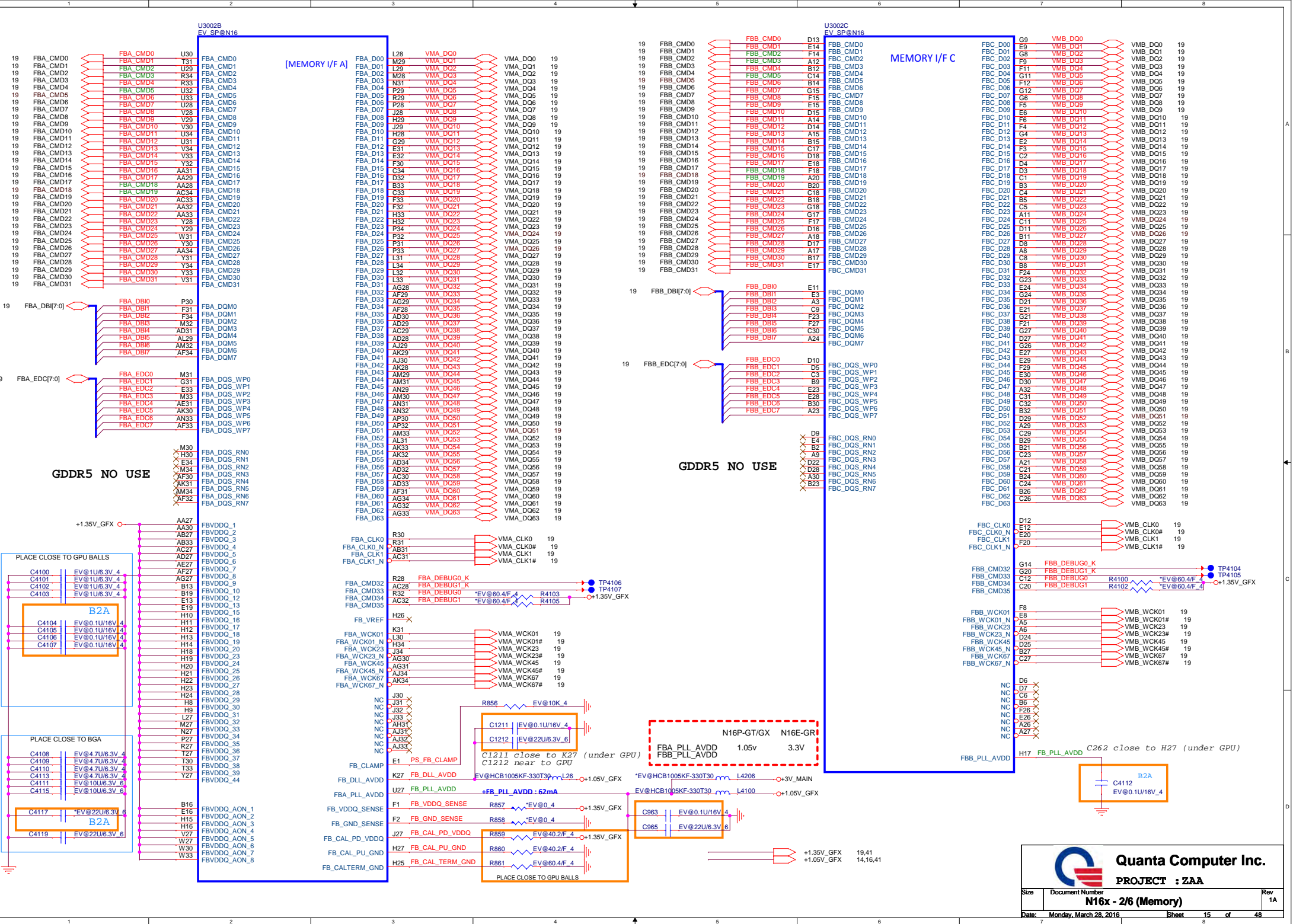
| | | |
|---|------------------------|----------------|
|  Quanta Computer Inc. PROJECT : ZAA | | Rev |
| | | 1A |
| Size | Document Number | |
| Skylake 10/17/18 (GND) | | |
| Date: | Monday, March 28, 2016 | Sheet 10 of 48 |



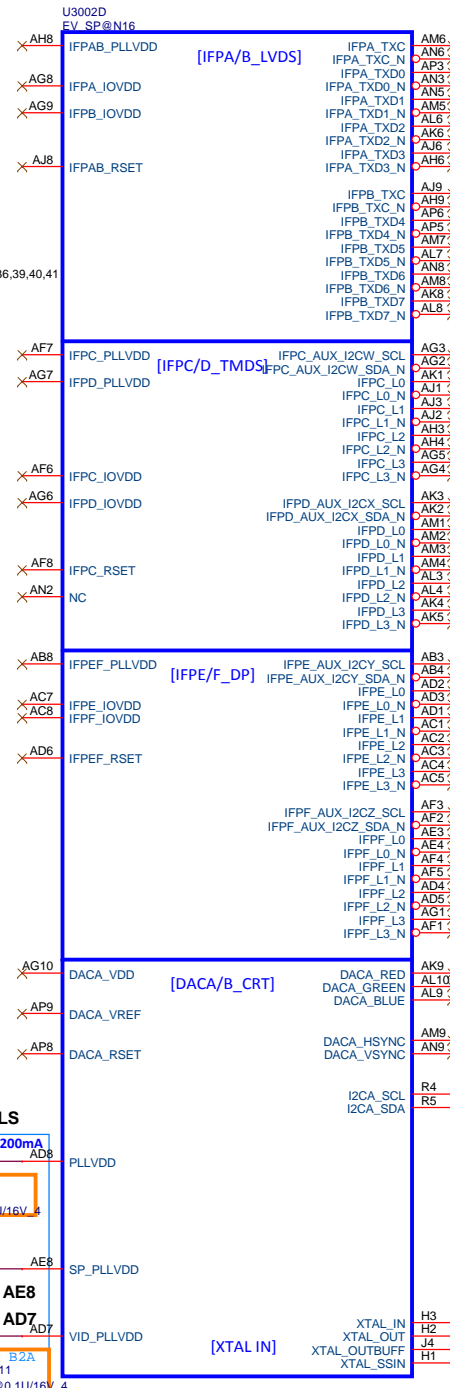
Intel APS Fixture use



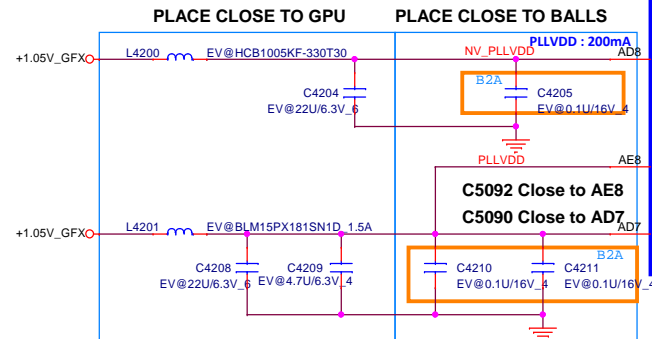
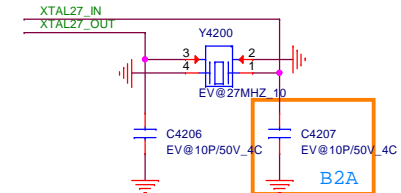
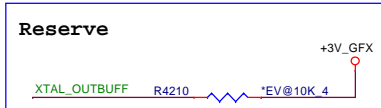
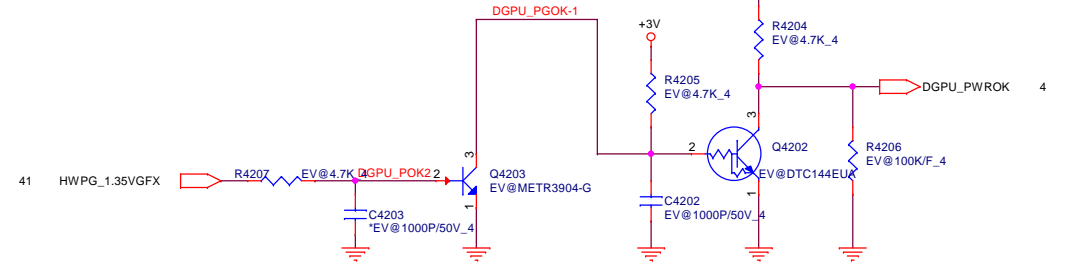
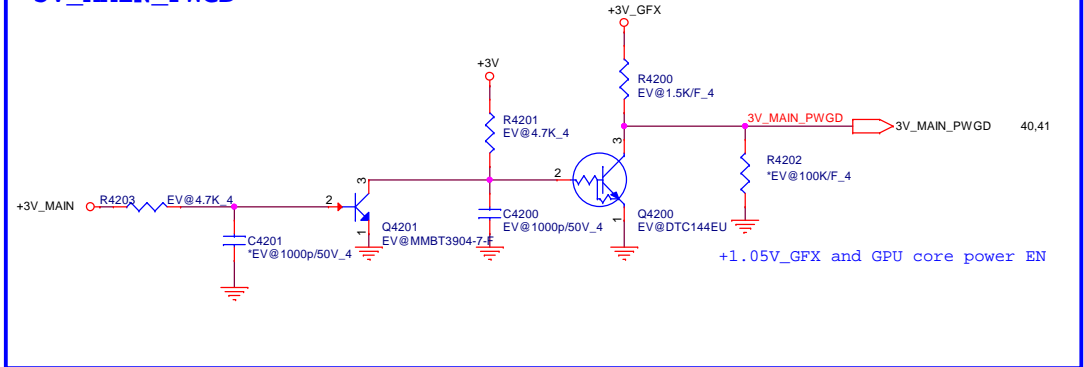


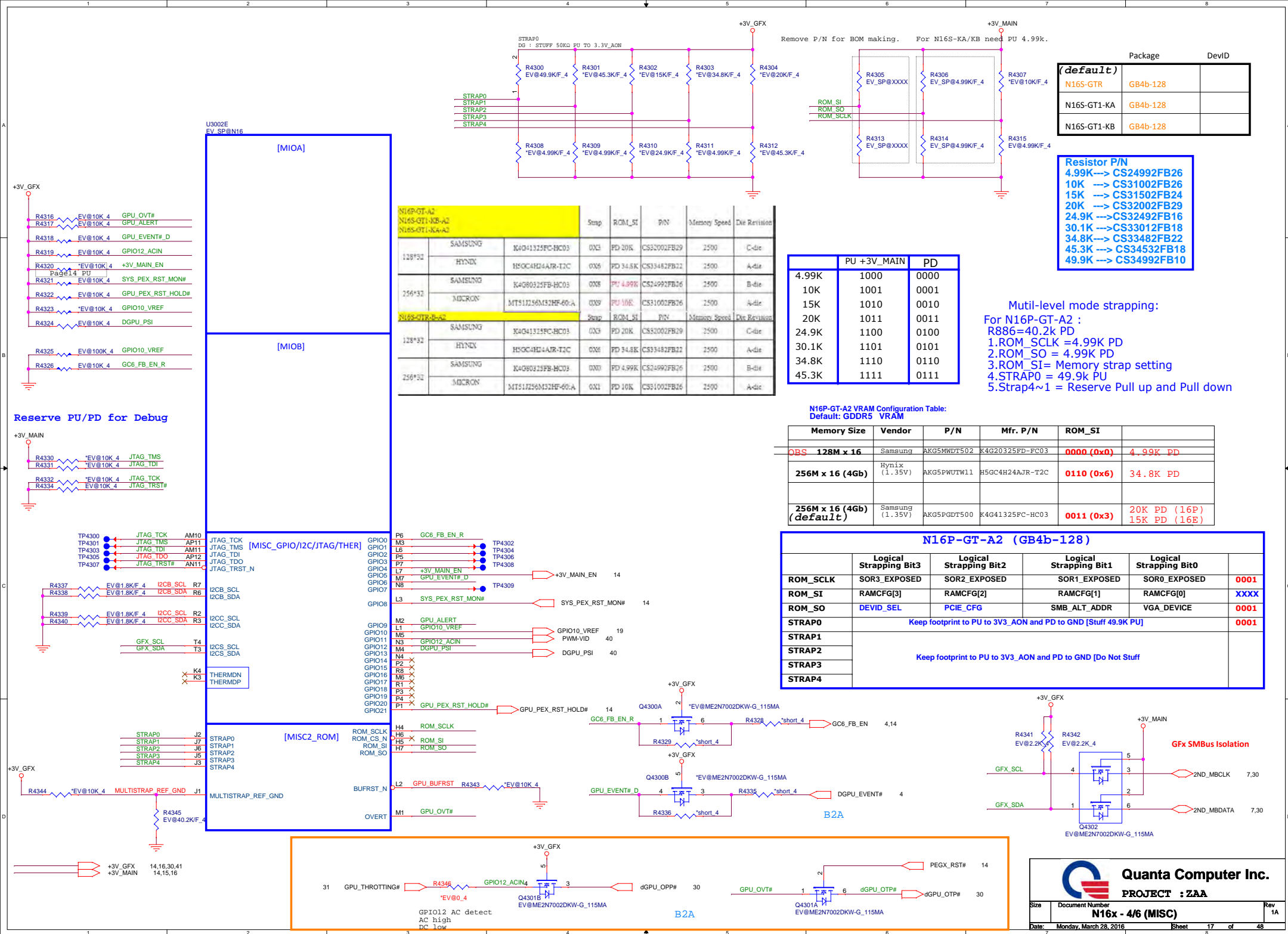


+3V_MAIN 14,15,17
 +1.05V_GFX 14,15,41
 +3V_GFX 14,17,30,41
 +3V 2,4,6,7,8,9,12,13,14,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41



3V_MAIN_PWGD





VDD/XVDD : 43A

+VGPU_CORE

U3002F
EV_SP@N16

[GPU VDD]

+VGPU_CORE

U3002G
EV_SP@N16

[GPU GND]

+VGPU_CORE

PLACE UNDER GPU

PLACE NEAR GPU



Quanta Computer Inc.

PROJECT : ZAA

| | | |
|------|------------------------|----------------|
| Size | Document Number | Rev |
| | N16x - 5/6 (Power) | 1A |
| Date | Monday, March 28, 2016 | Sheet 18 of 48 |

CHANNEL A: 1024MB GDDR5x32

Non-mirror, MF=0
Channel A
<0-31>

Mirror, MF=1
Channel A
<32-63>

Non-mirror, MF=0
Channel B
<0-31>

Mirror, MF=1
Channel B
<32-63>

DQA24~31

DQA16~23

DQA8~15

DQA0~7

DQA32~39

DQA40~47

DQA48~55

DQA56~63

DQB24~31

DQB16~23

DQB8~15

DQB0~7

DQB32~39

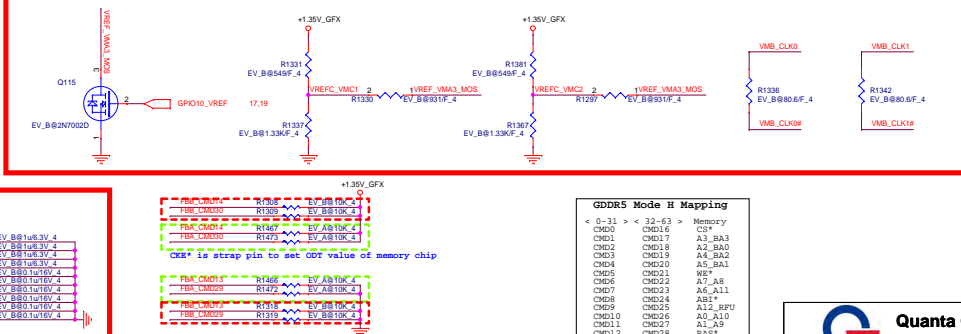
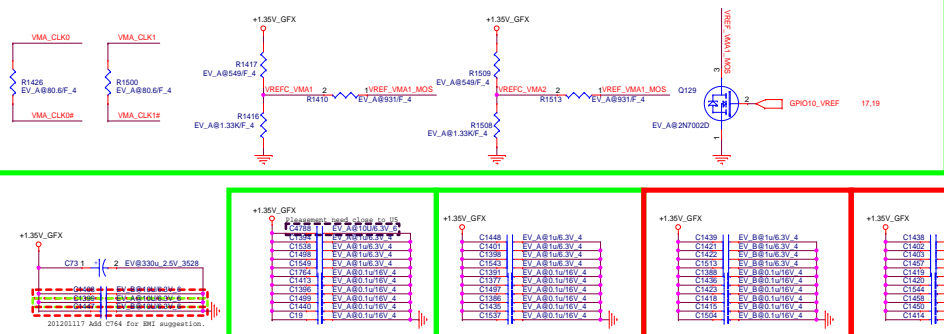
DQB40~47

DQB48~55

DQB56~63

KB OnlyA

KA OnlyB

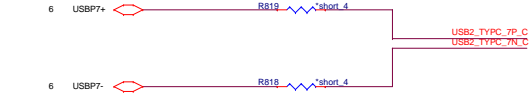


GDDR5 Mode H Mapping

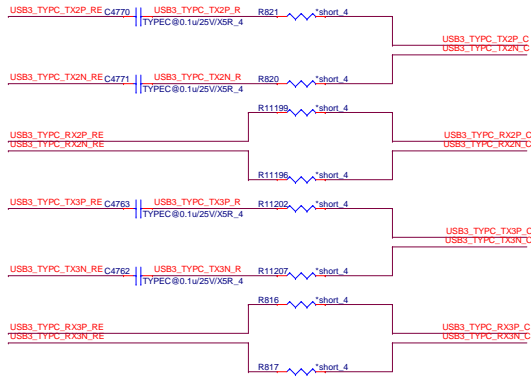
| < 0-31 > | < 32-63 > | Memory |
|----------|-----------|----------|
| CH00 | CH16 | C8* |
| CH01 | CH17 | A3, BA3 |
| CH02 | CH18 | A2, BA2 |
| CH03 | CH19 | A4, BA4 |
| CH04 | CH20 | A5, BA5 |
| CH05 | CH21 | W8* |
| CH06 | CH22 | A7, A8 |
| CH07 | CH23 | A6, A11 |
| CH08 | CH24 | AB1* |
| CH09 | CH25 | A12, RPU |
| CH10 | CH26 | A0, A10 |
| CH11 | CH27 | A1, A9 |
| CH12 | CH28 | B3* |
| CH13 | CH29 | R2* |
| CH14 | CH30 | CKE* |
| CH15 | CH31 | CA5* |

USB TYPE-C

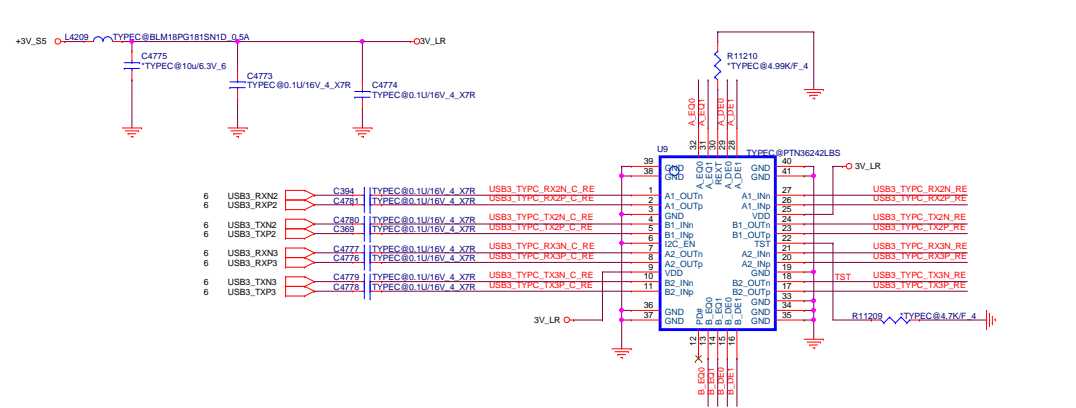
USB2.0 ESD



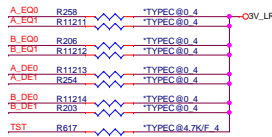
Type C1 HSIO ESD



USB3 Re-Driver

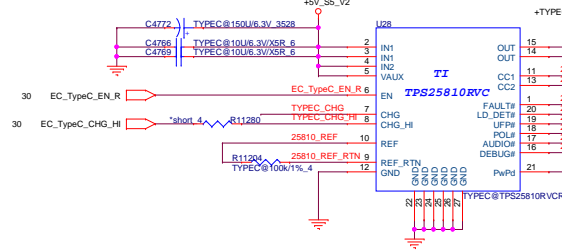


| A_EQ0 | A_EQ1 | A_DE0 | A_DE1 | |
|-------|-------|-------|-------|----------------|
| B_EQ0 | B_EQ1 | B_DE0 | B_DE1 | |
| 0 | 0 | 9dB | 0 | -3.5dB |
| 0 | 1 | 3dB | 0 | no de-emphasis |
| 1 | 0 | 6dB | 1 | -7dB |
| 1 | 1 | 7.5dB | 1 | -5dB |

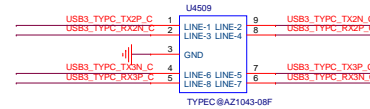
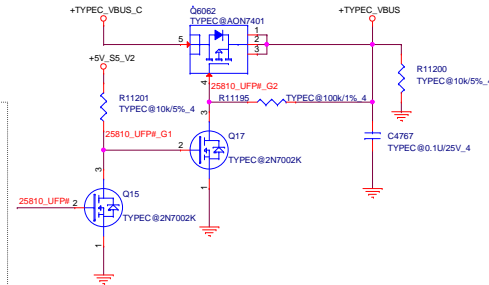


TST: Low = Normal LFPS swing / High = Turn down LFPS swing

Vendor suggest input cap 120u



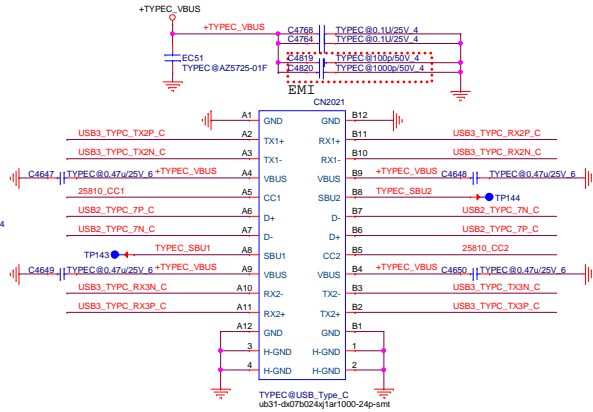
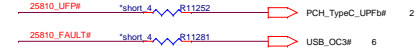
| TPS25810 Part | CC1 | CC2 | OUT | VCON (mV) | POL | UFPs | AUDIOs | DEBUds |
|-----------------------------------|------|------|------|-----------|-----|------|--------|--------|
| Seating Attached | OPEN | OPEN | OPEN | CC1 | H-Z | H-Z | H-Z | H-Z |
| UFP Connected | RA | OPEN | INT | NO | H-Z | LOW | H-Z | H-Z |
| Powered Cable/No UFP Connected | OPEN | RA | INT | NO | LOW | LOW | H-Z | H-Z |
| Powered Cable/No UFP Connected | OPEN | RA | OPEN | NO | H-Z | LOW | H-Z | H-Z |
| Powered Cable/UFP Connected | RA | OPEN | CO2 | NO | H-Z | LOW | H-Z | H-Z |
| Powered Cable/UFP Connected | RA | INT | CO1 | NO | LOW | LOW | H-Z | H-Z |
| Powered Cable/UFP Connected | RA | INT | CO2 | NO | LOW | LOW | H-Z | H-Z |
| Debiting Accessory Connected | RA | RA | OPEN | NO | H-Z | H-Z | LOW | H-Z |
| Audio Adapter Accessory Connected | RA | RA | OPEN | NO | H-Z | H-Z | LOW | H-Z |



Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00AZ5725-01F.R7G0.009 PD 5V (follow ZAA)



| CC1 | CC2 | CC Capacity | Current Limit | Load Switch |
|-----|-----|-------------|---------------|-------------|
| 0 | 0 | 1.5nF | 1.5A | NA |
| 0 | 1 | 1.5nF | 1.5A | NA |
| 1 | 0 | 1.5nF | 1.5A | NA |
| 1 | 1 | 1.5nF | 1.5A | NA |



Quanta Computer Inc.

PROJECT : ZAA

Size Document Number

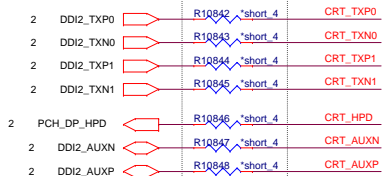
USB Type C 25810

Date Monday, March 28, 2016 Sheet 20 of 48

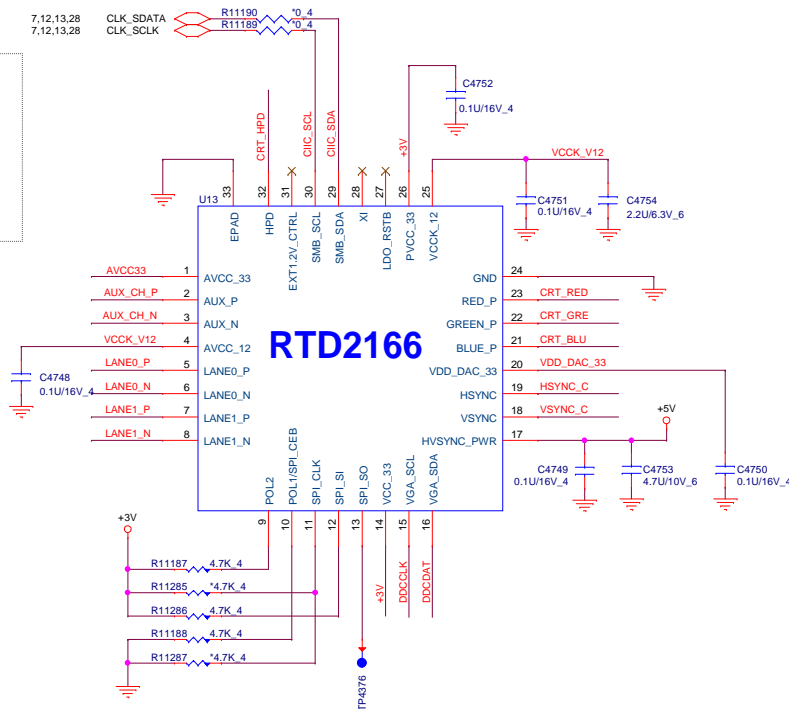
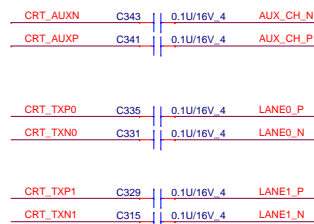
Rev 1A

DP TO VGA

Close to CPU side of CAP.



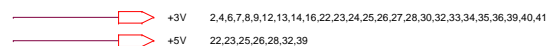
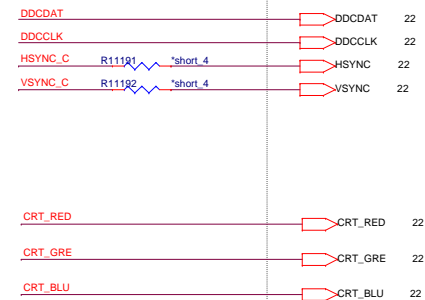
Power



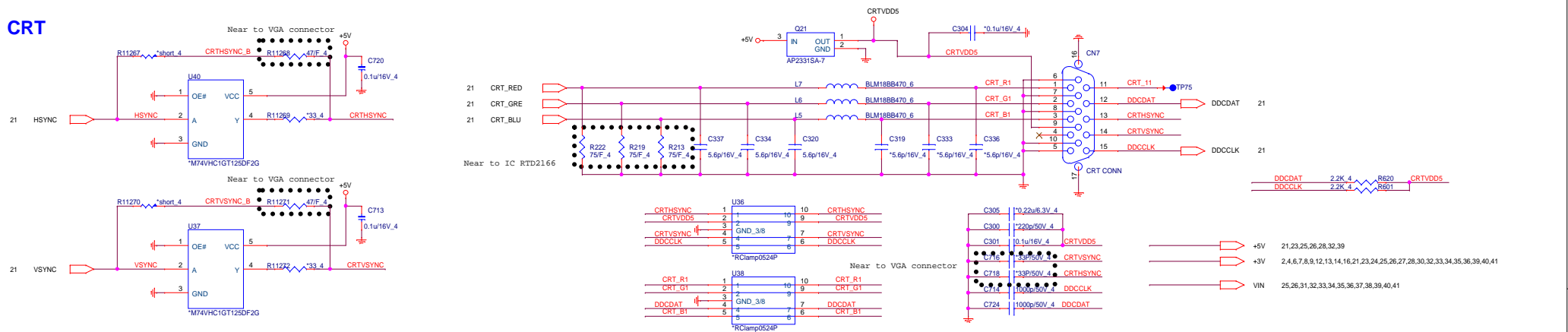
Note:

- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 shold be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

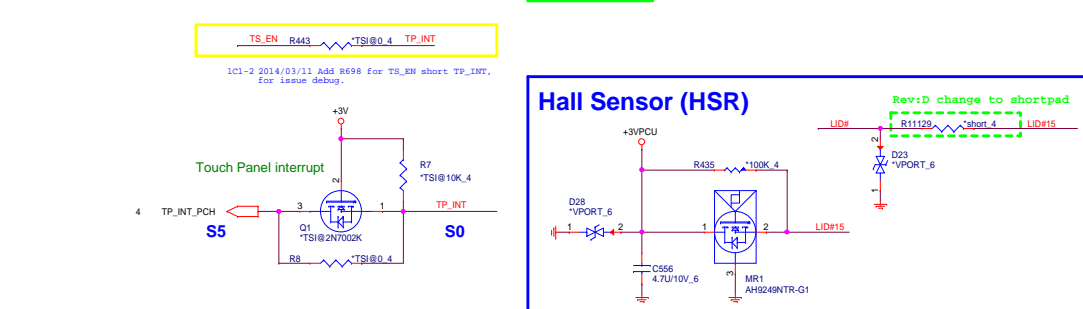
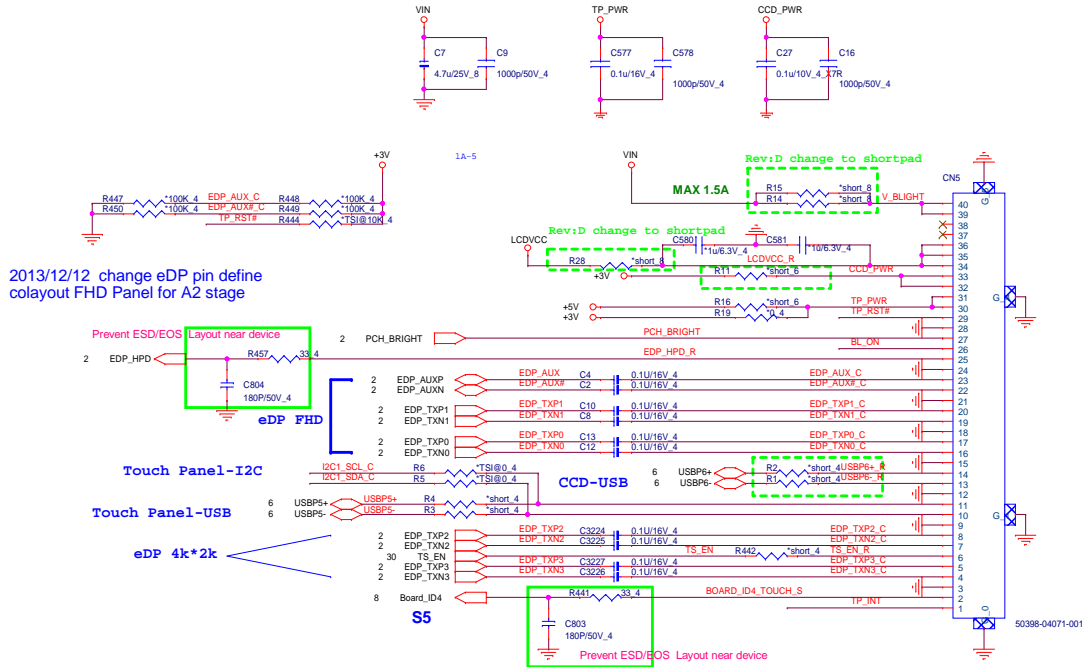
VGA



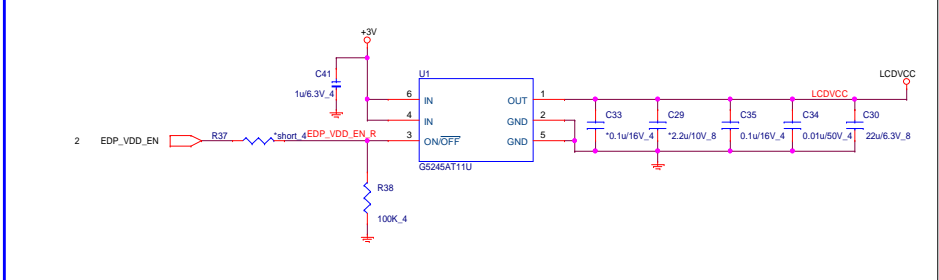
CRT



LCD CONNECTOR



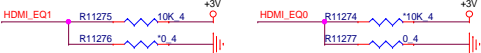
LCD Power



Touch screen level shift I2C(res

HDMI

| OE_N | DDC_EN | HPD_SINK | Source output | PTN3366 power mode |
|------|--------|------------|---------------|-------------------------|
| LOW | HIGH | HIGH | source active | Active mode; DDC active |
| LOW | LOW | LOW | don't care | Standby mode |
| HIGH | LOW | don't care | don't care | Ultra low-power mode |

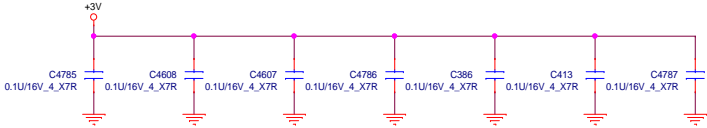
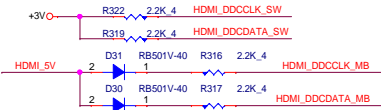
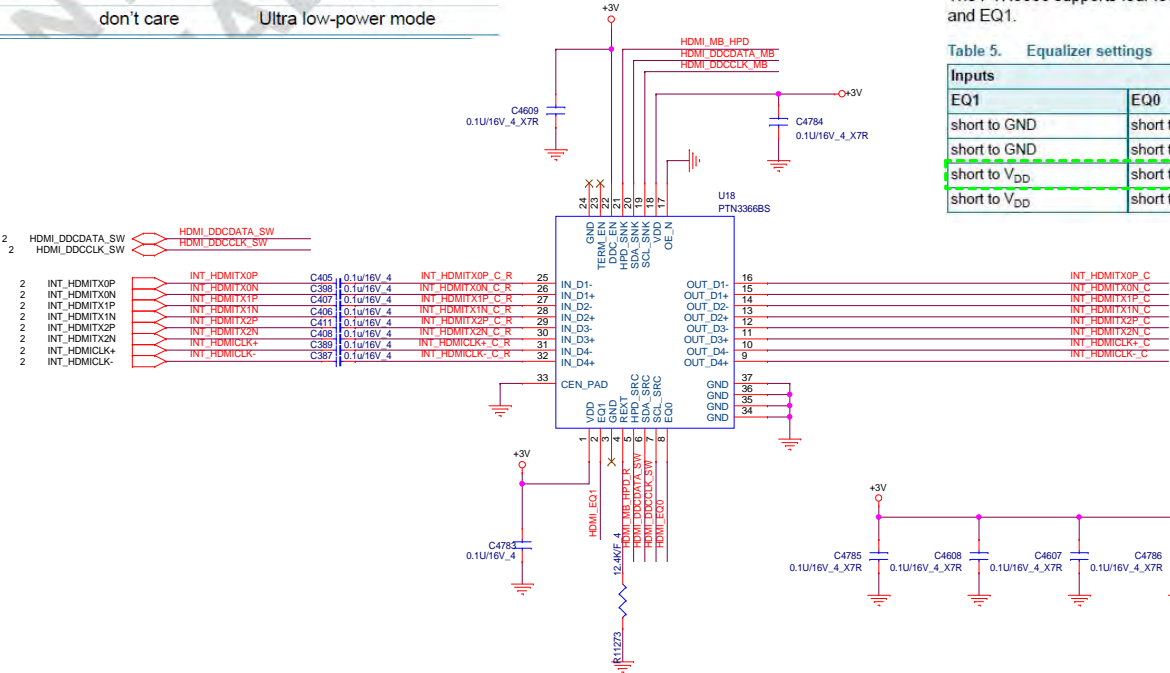


The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

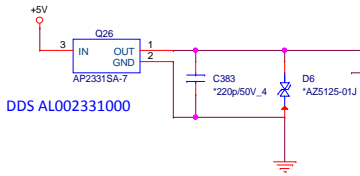
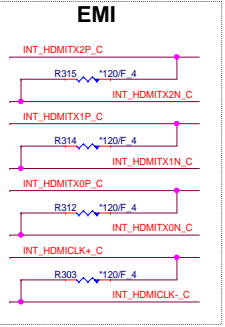
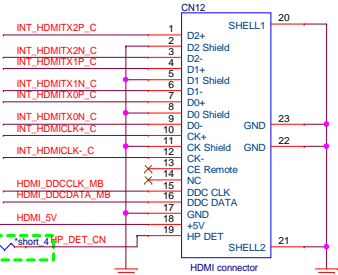
Table 5. Equalizer settings

| Inputs | | Equalization for 3 Gbit/s |
|--------------|--------------|---------------------------|
| EQ1 | EQ0 | |
| short to GND | short to GND | 0 dB |
| short to GND | short to VDD | 2 dB |
| short to VDD | short to GND | 4 dB |
| short to VDD | short to VDD | 6 dB |

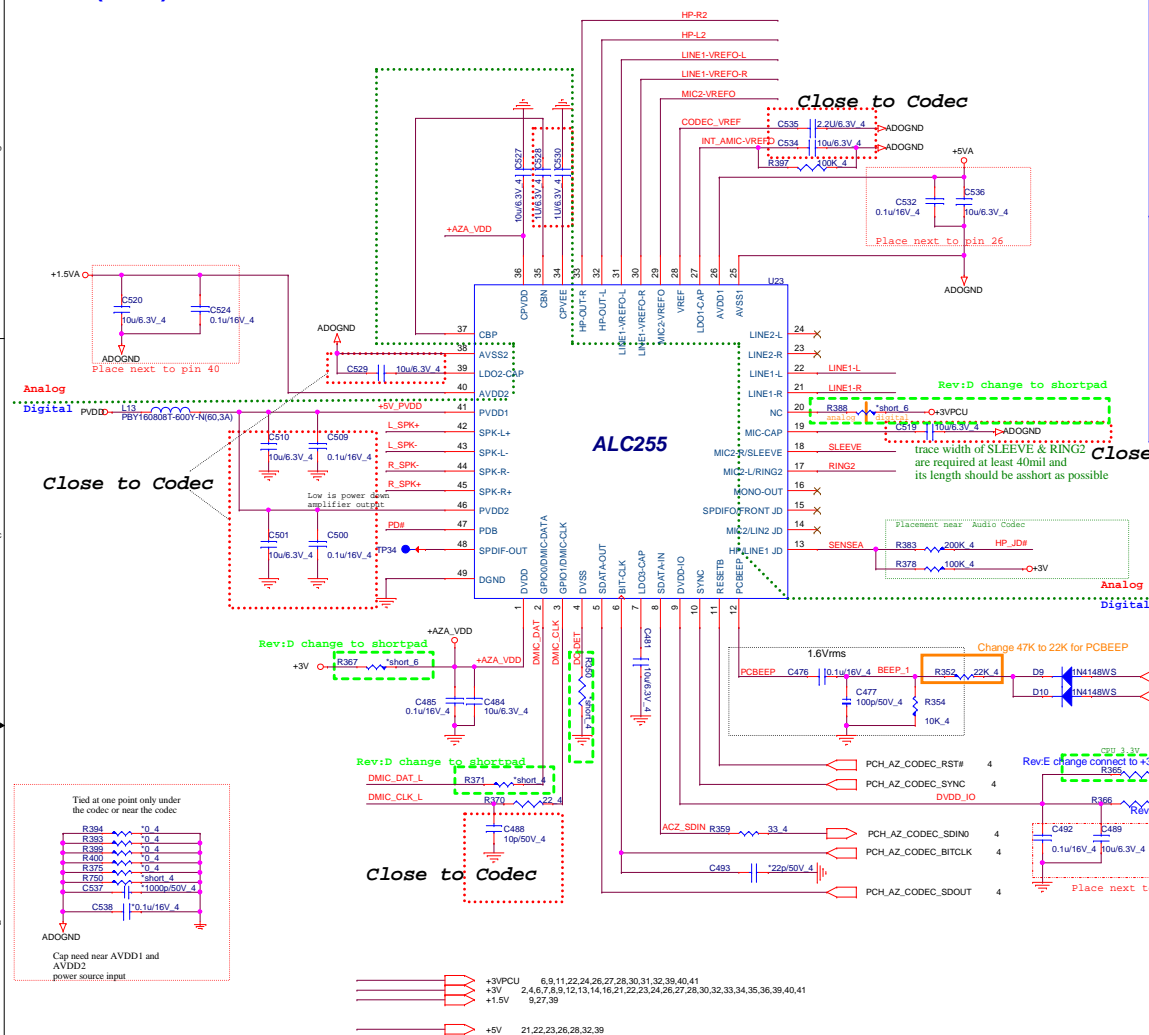
From PCH



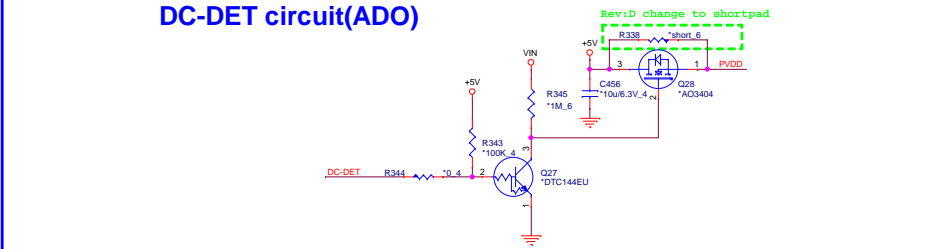
HDMI connector



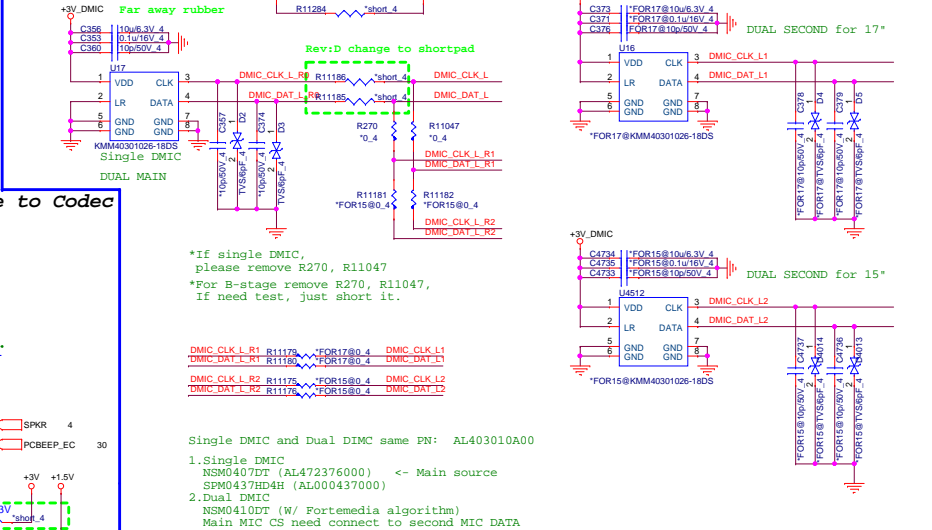
Codec(ADO)



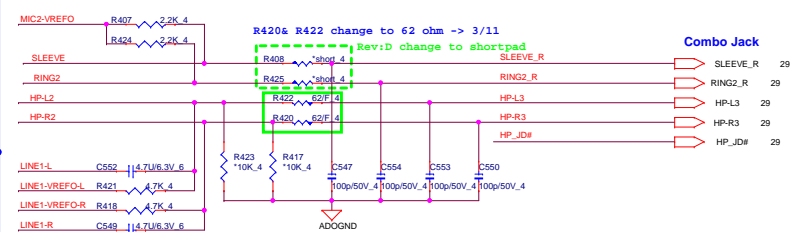
DC-DET circuit(ADO)



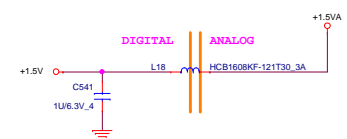
D-Mic (MIC)



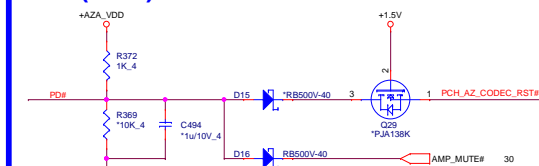
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



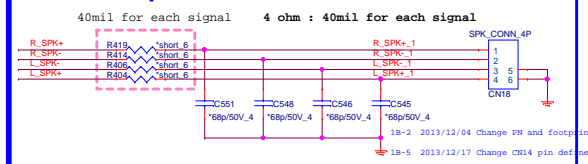
Codec PWR 1.5V(ADO)



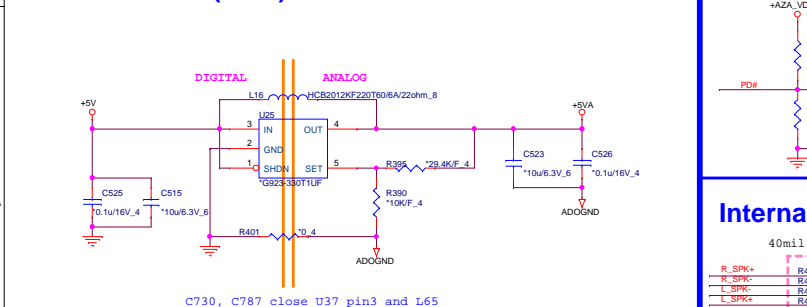
Mute(ADO)



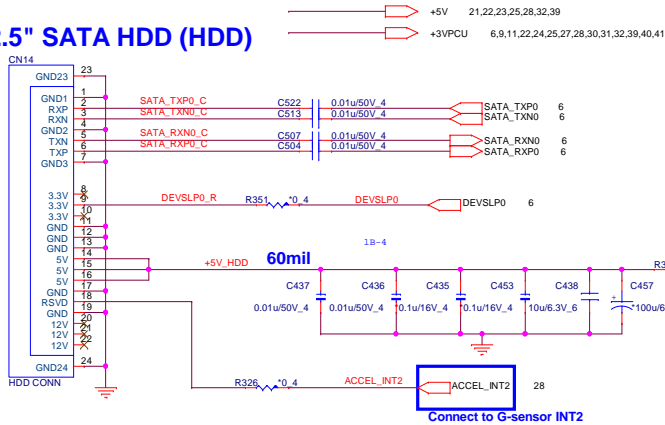
Internal Speaker



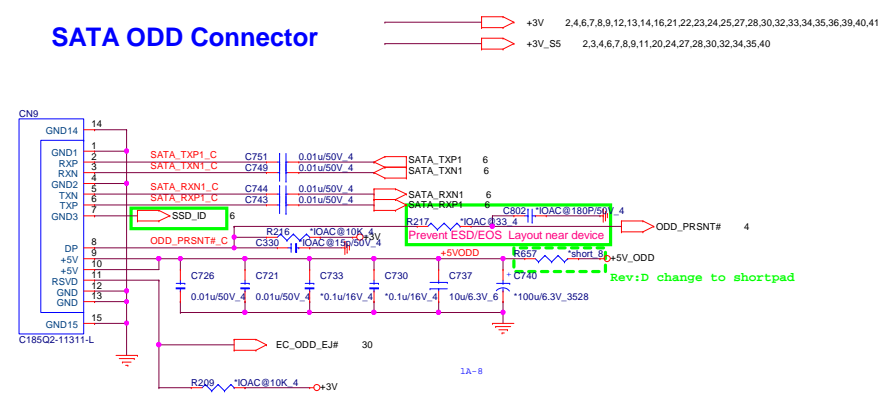
Codec PWR 5V(ADO)



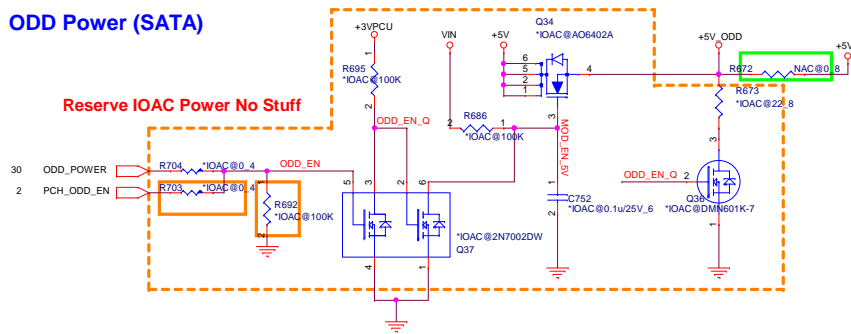
2.5" SATA HDD (HDD)



SATA ODD Connector



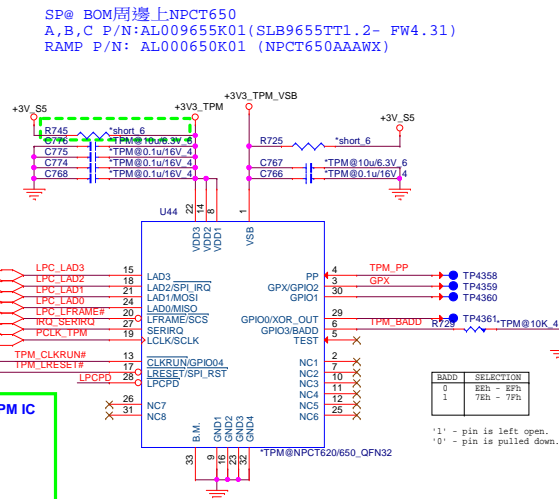
ODD Power (SATA)



TPM NPCT650 (TPM)

AL000650K01 :NPCT650AAAWX

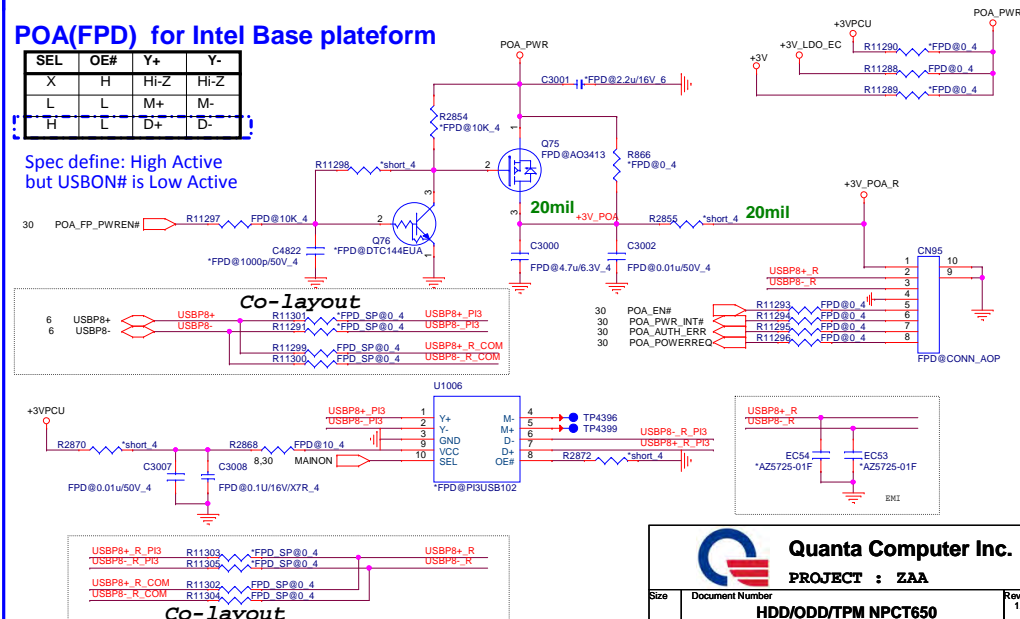
| | |
|----------|--------------|
| TPMM 1.2 | AL0009655K01 |
| TPMM 2.0 | AL000650K01 |



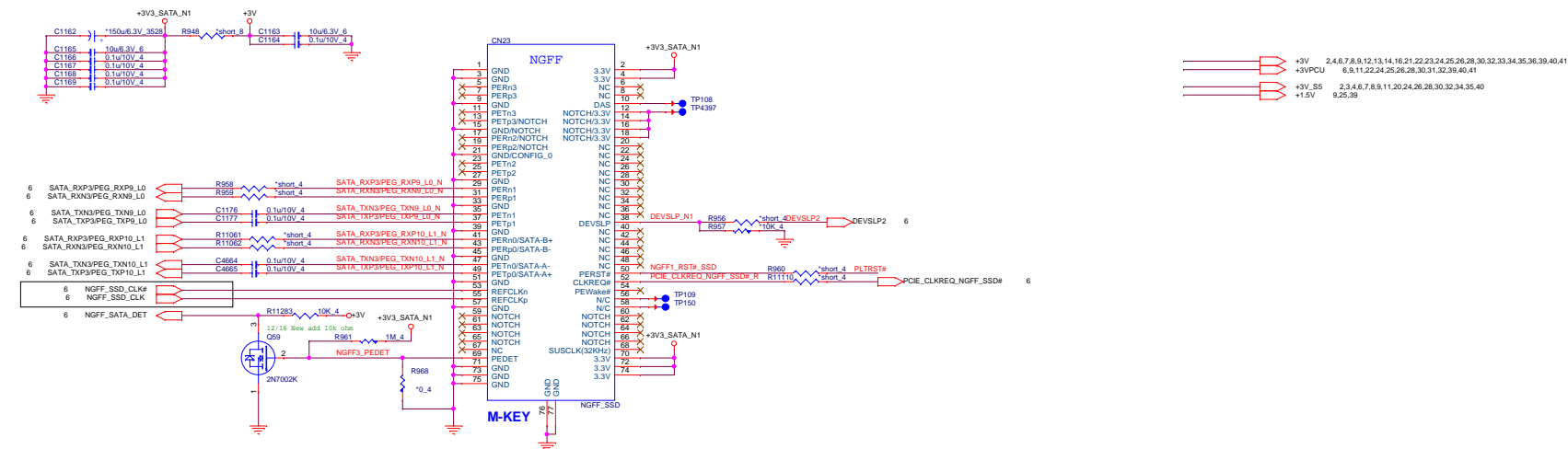
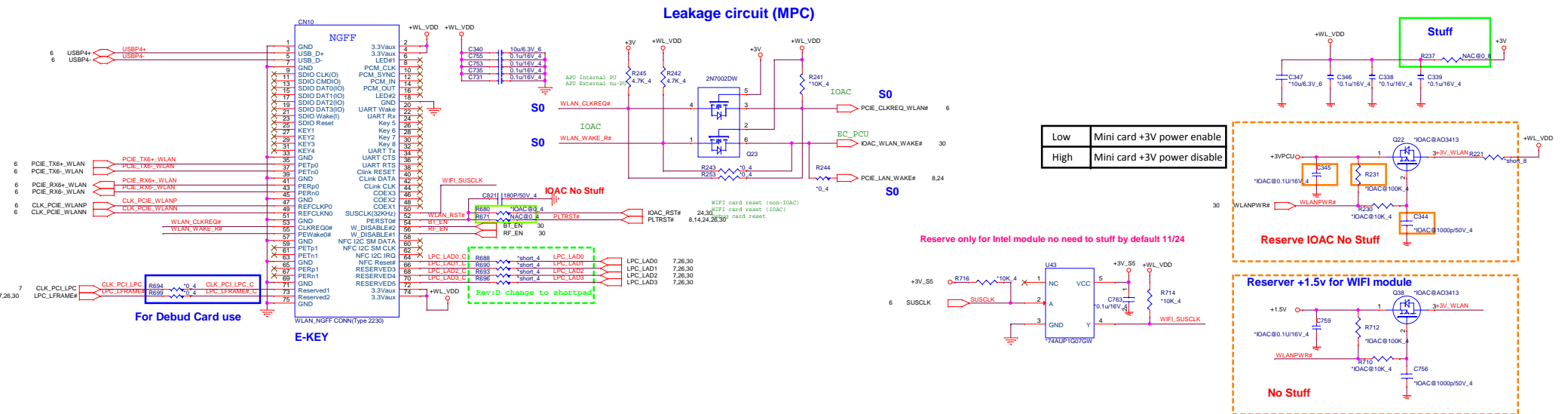
POA(FPD) for Intel Base platfrom

| SEL | OE# | Y+ | Y- |
|-----|-----|------|------|
| X | H | Hi-Z | Hi-Z |
| L | L | M+ | M- |
| H | L | D+ | D- |

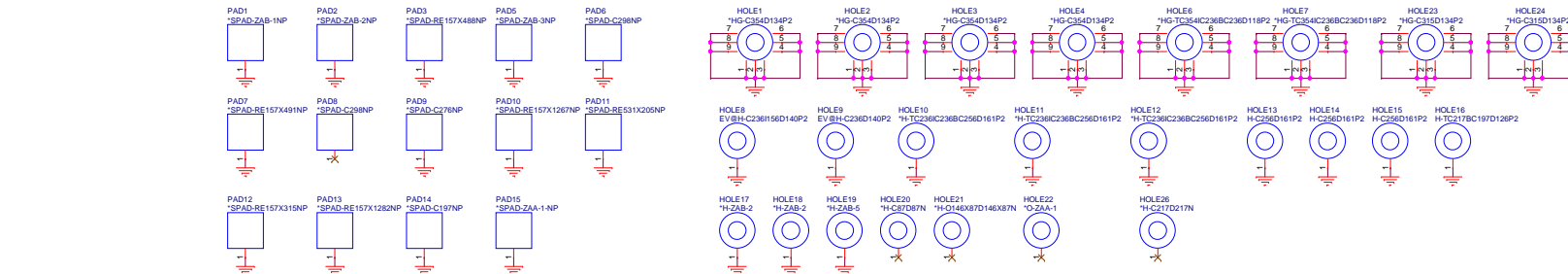
Spec define: High Active
but USBON# is Low Active



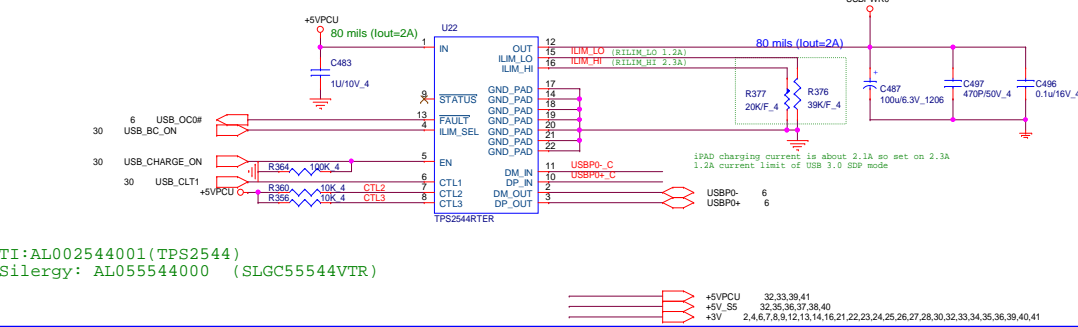
NGFF_M.2 WiFi & BT (NGF)



PAD and HOLE



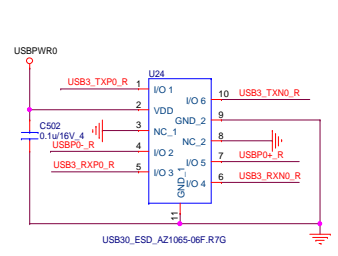
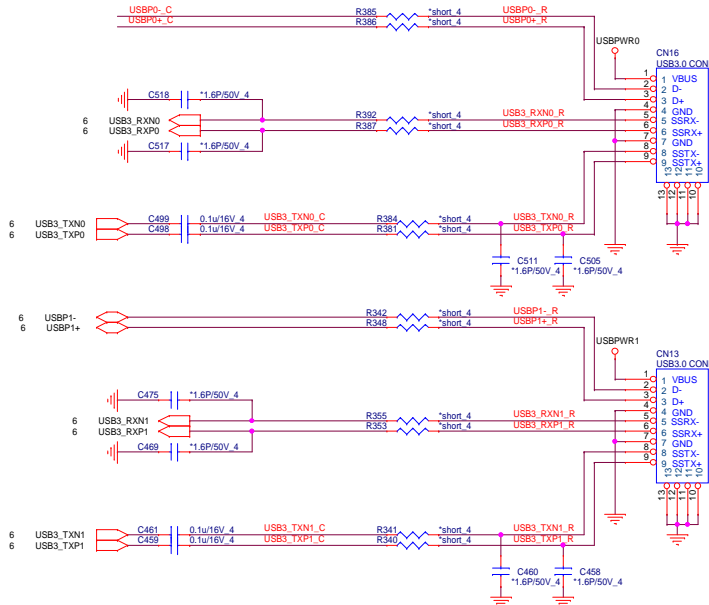
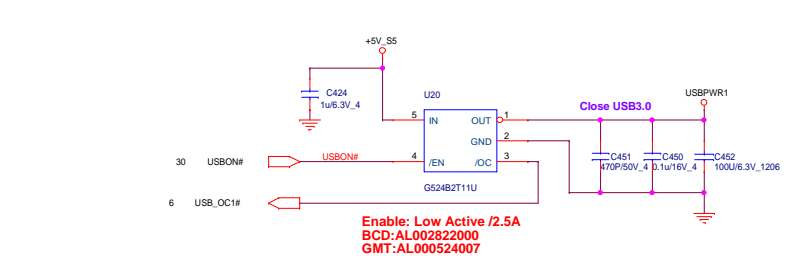
USB Charger to 3.0 (UBC)



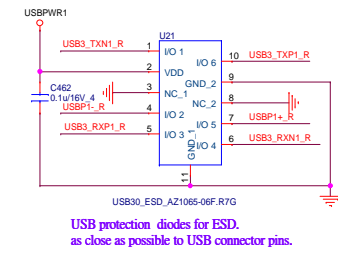
| | CTL1 | CTL2 | CTL3 | ILIM_SEL |
|-----|------|------|------|----------|
| SDP | 1 | 1 | 1 | 0 |
| CDP | 1 | 1 | 1 | 1 |
| DCP | 0 | 1 | 1 | X |

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1) $IOS_typ(mA) = 50,250 / (RILIM_XX(K\Omega) + 0.1)$
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

USB 3.0 Connector (UB3)

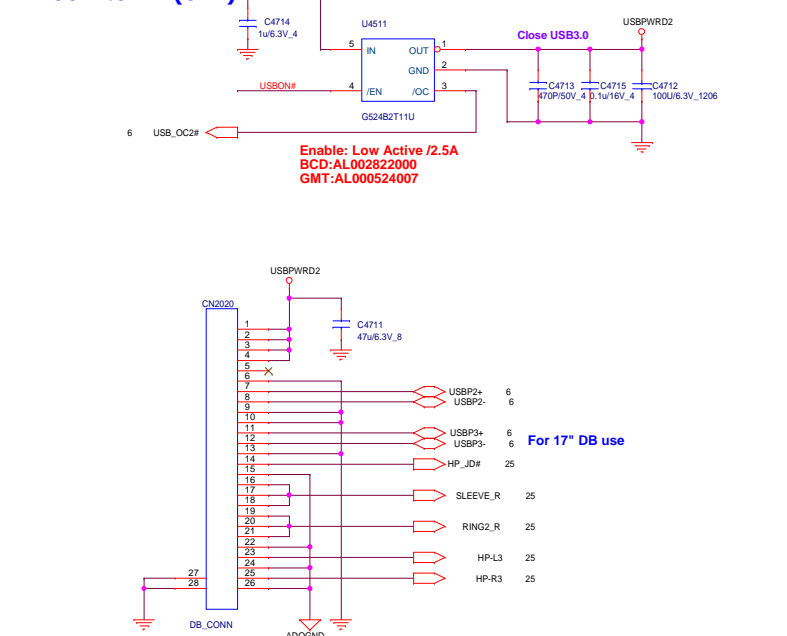


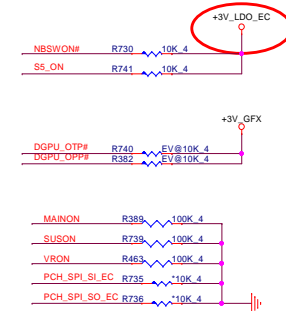
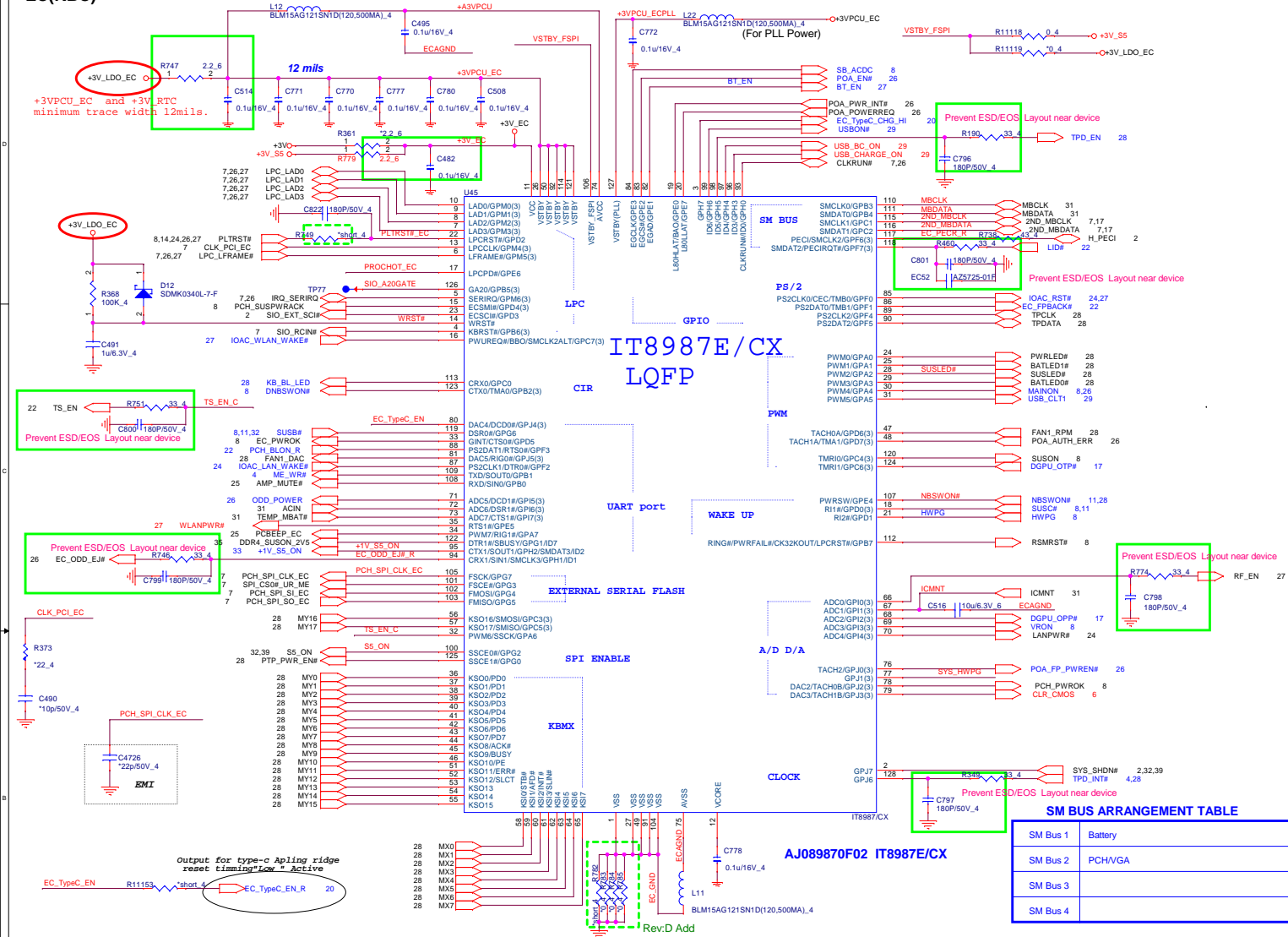
USB protection diodes for ESD, as close as possible to USB connector pins.



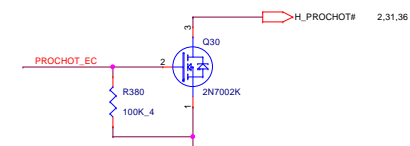
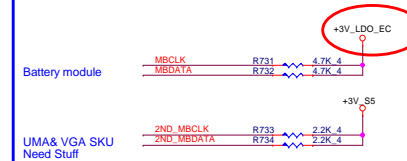
USB protection diodes for ESD, as close as possible to USB connector pins.

USB2.0 DB (UB2)

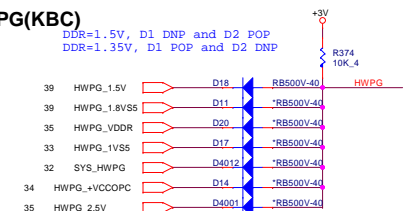




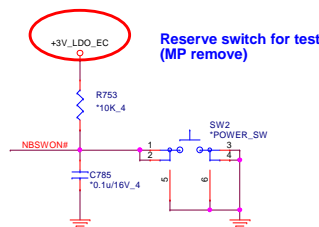
SM BUS PU(KBC)



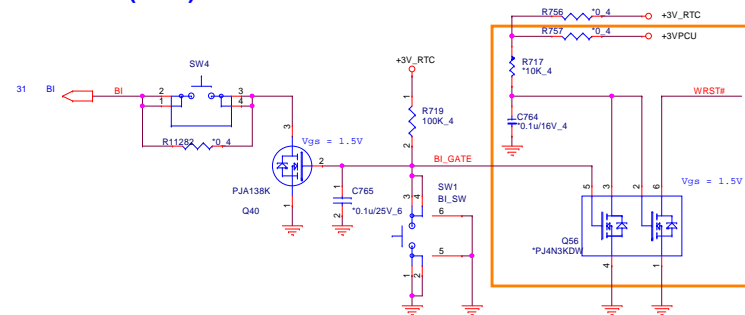
HWPG(KBC)



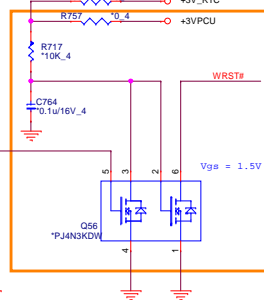
| | |
|----------|---------|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH/VGA |
| SM Bus 3 | |
| SM Bus 4 | |



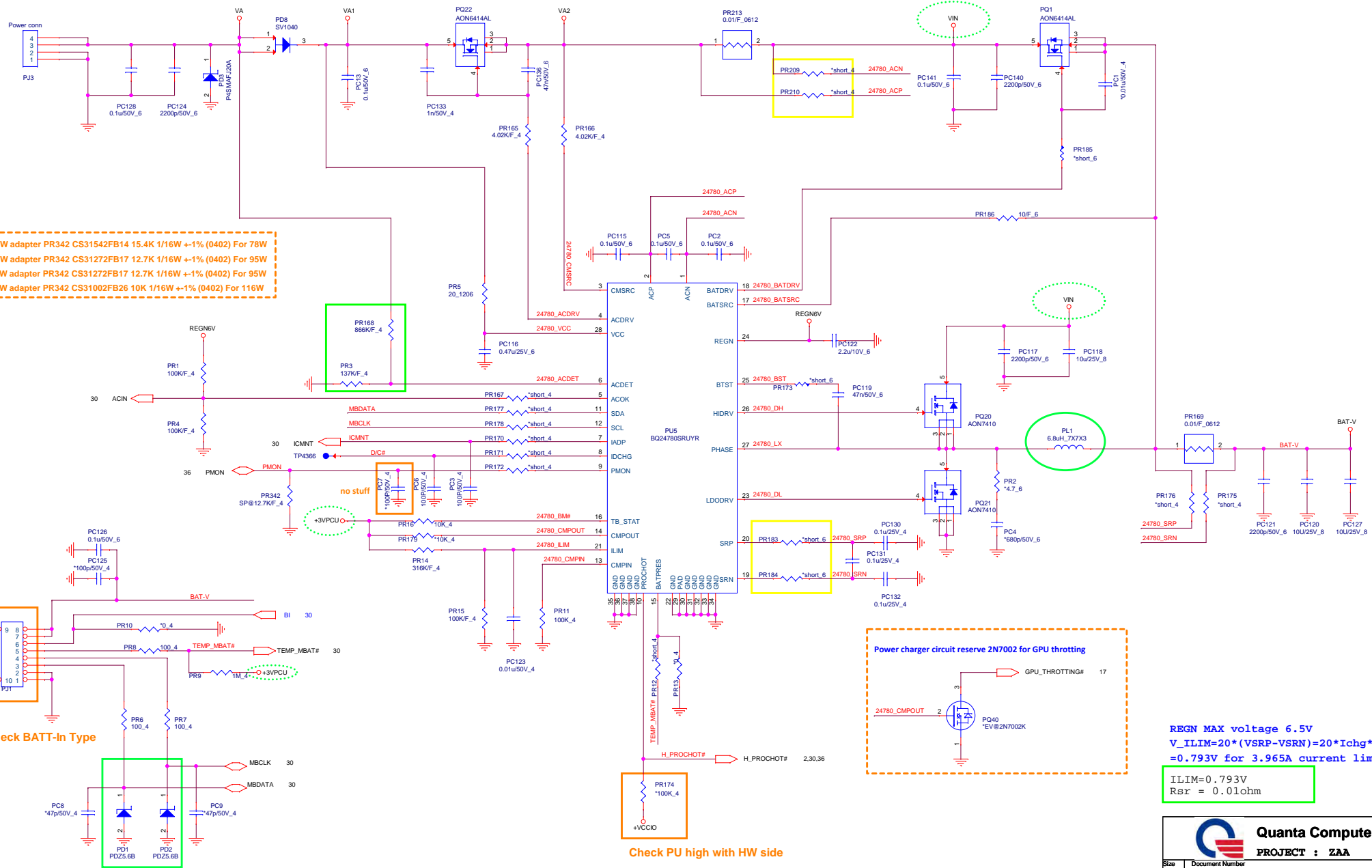
Reset SW (FSW)

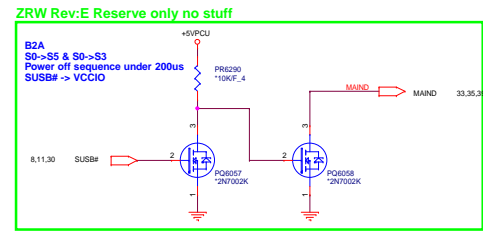
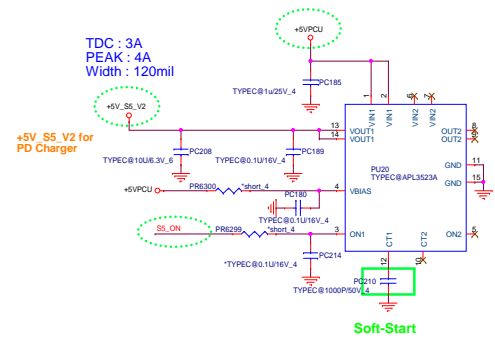
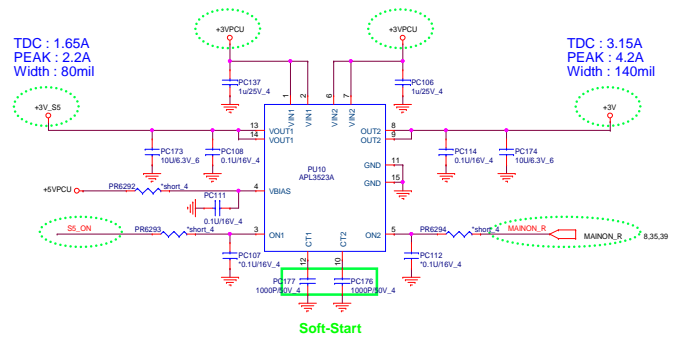
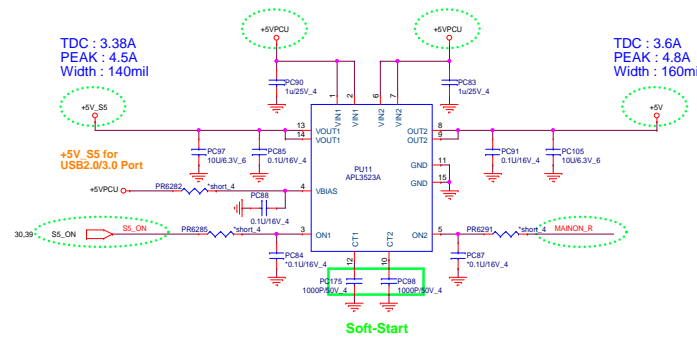
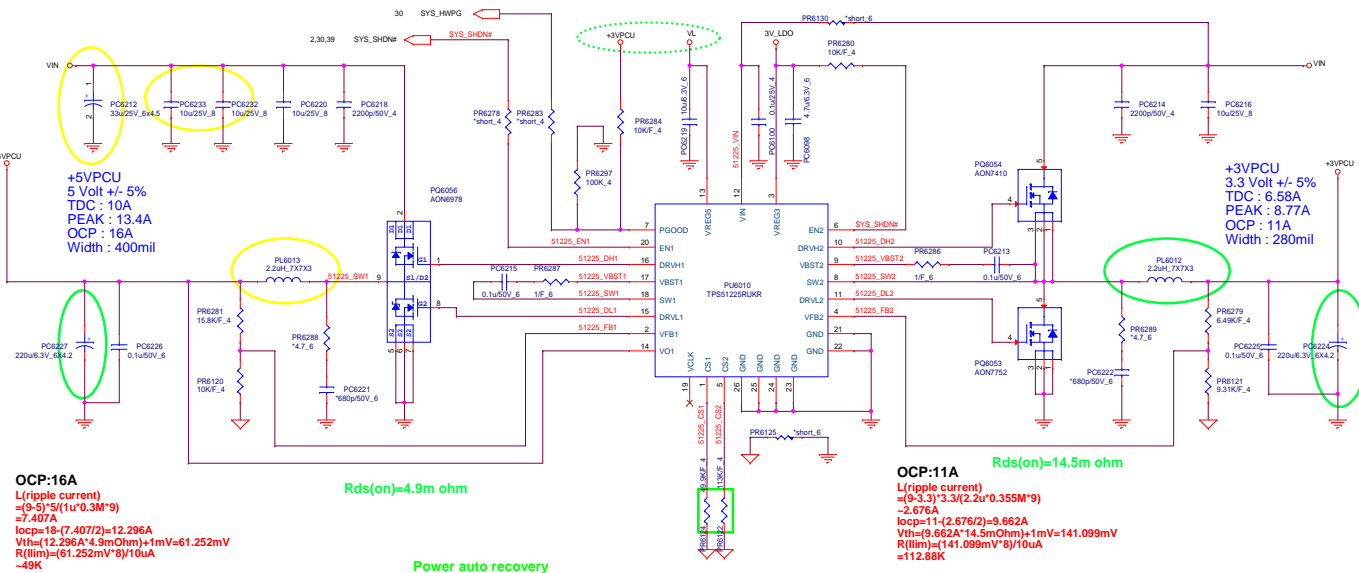


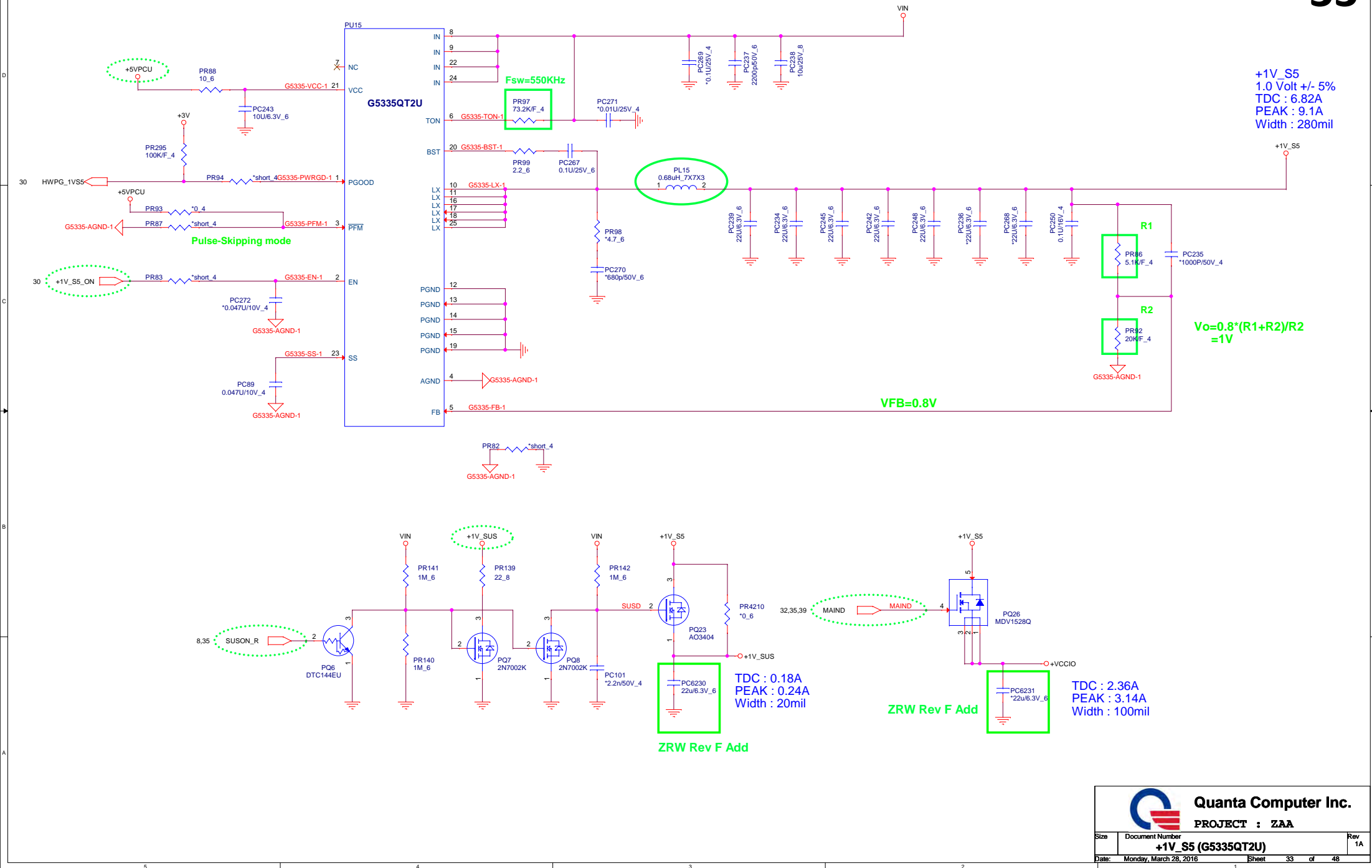
Battery Detect Switch



Double Check ADP-In Type

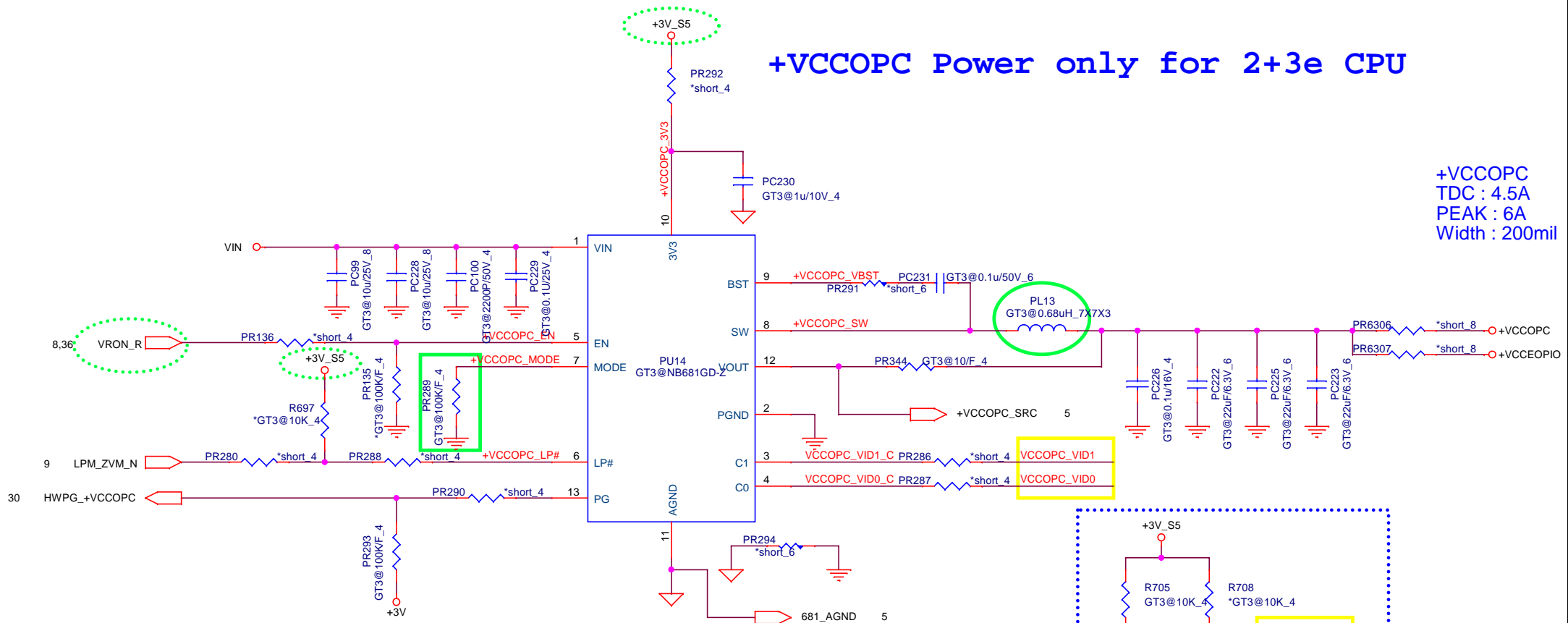






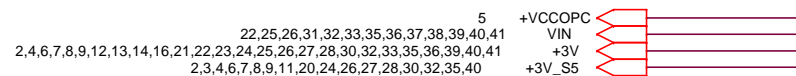
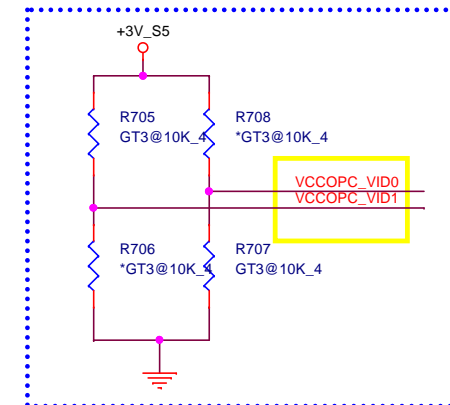
+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



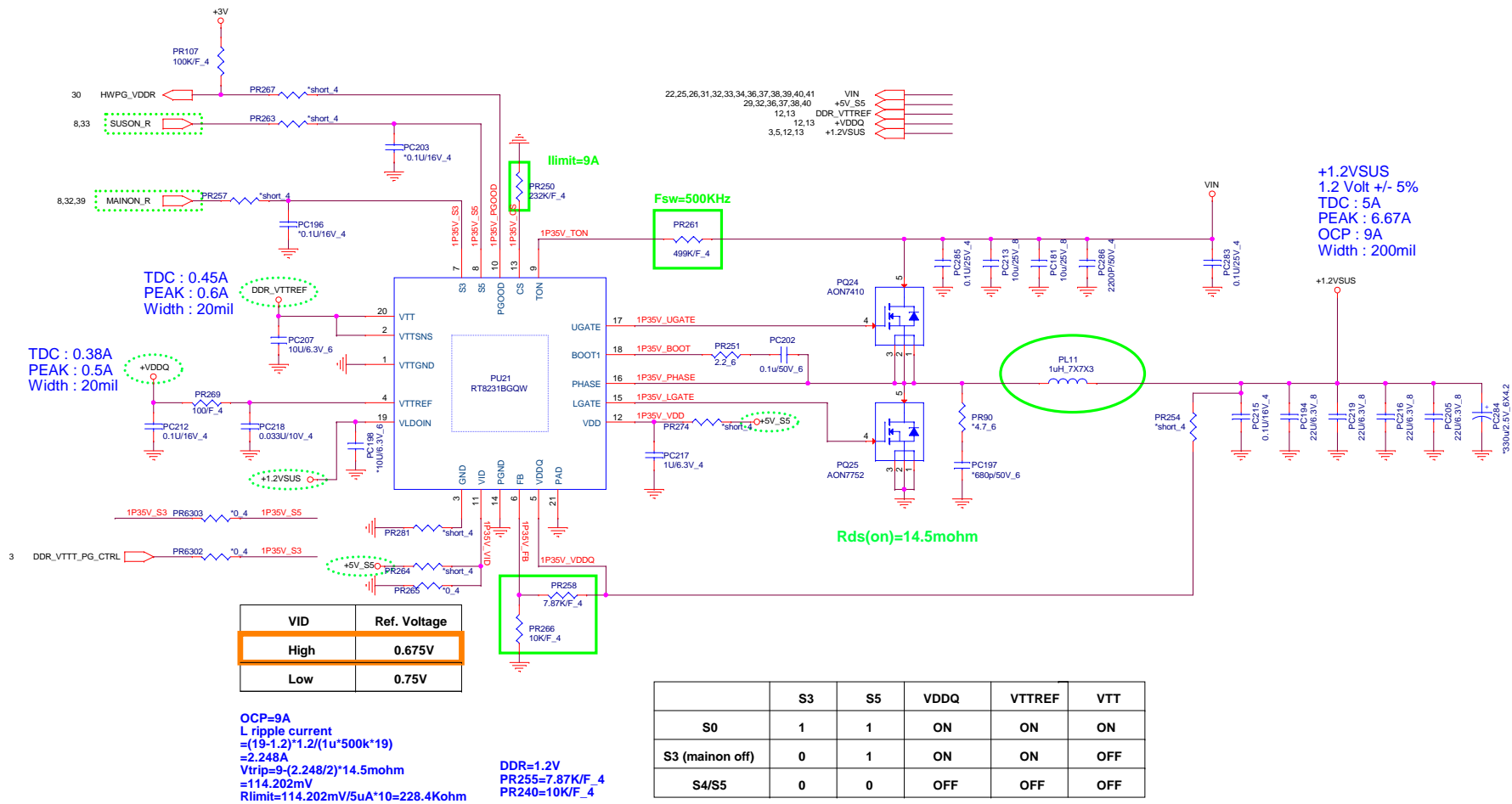
| Mode | VR Rail |
|----------|-------------|
| 0 ohm | VCCIO |
| Floating | PRIMCORE |
| 100K | EDRAM/EOPIO |
| 150K | Other |

| | LP# | C1 | C0 | Vo |
|----------|-----|----|----|-----------|
| VCCEDRAM | 0 | X | X | 0V |
| | 1 | 0 | 0 | 0.8V(MSM) |
| | 1 | 0 | 1 | 0.95V |
| | 1 | 1 | 0 | 1.0V |
| | 1 | 1 | 1 | 1.05V |

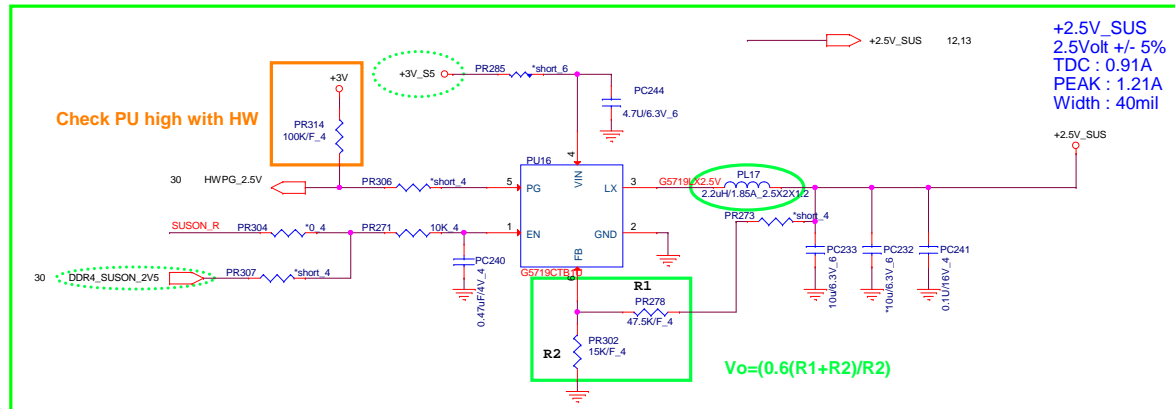


Quanta Computer Inc.
PROJECT : ZAA

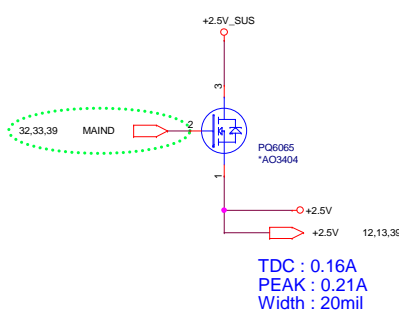
| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | +VCCOPC (NB681GD-Z) | 1A |
| Date: | Monday, March 28, 2016 | Sheet 34 of 48 |



+2.5VSUS Power Rail For DDR4

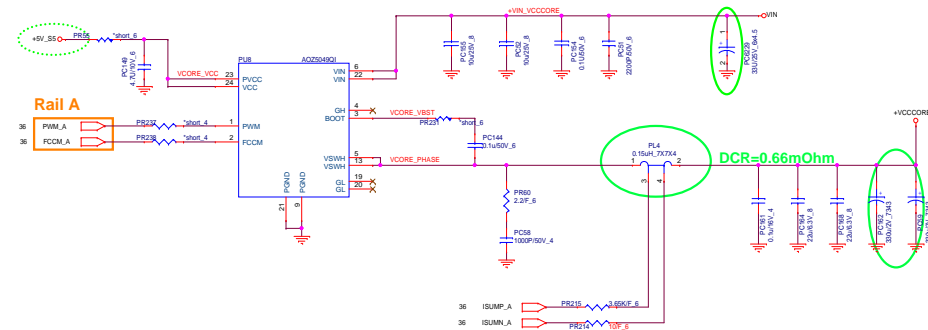


10/26 Reserve +2.5V for DDR4 VDDSPD



GT2: PR19 Unstuff
GT3: PR19 CS41003F932 100K

VCORE



VCORE

Icc TDC PL2 : 23A

Icc Max : 32A

OCF : 35A

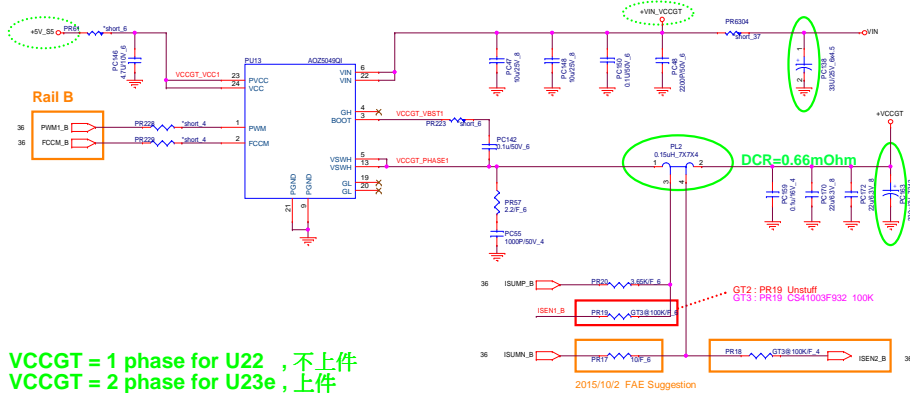
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

Icc TDC PL2 : 40A

Icc Max : 64A

OCF : A

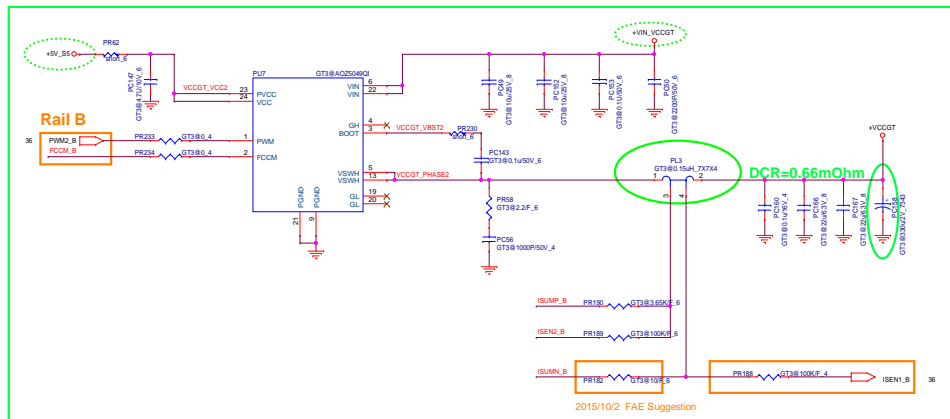
Fsw : 800KHz

VCCGT L/L :

R_DC_LL : 2mV/A

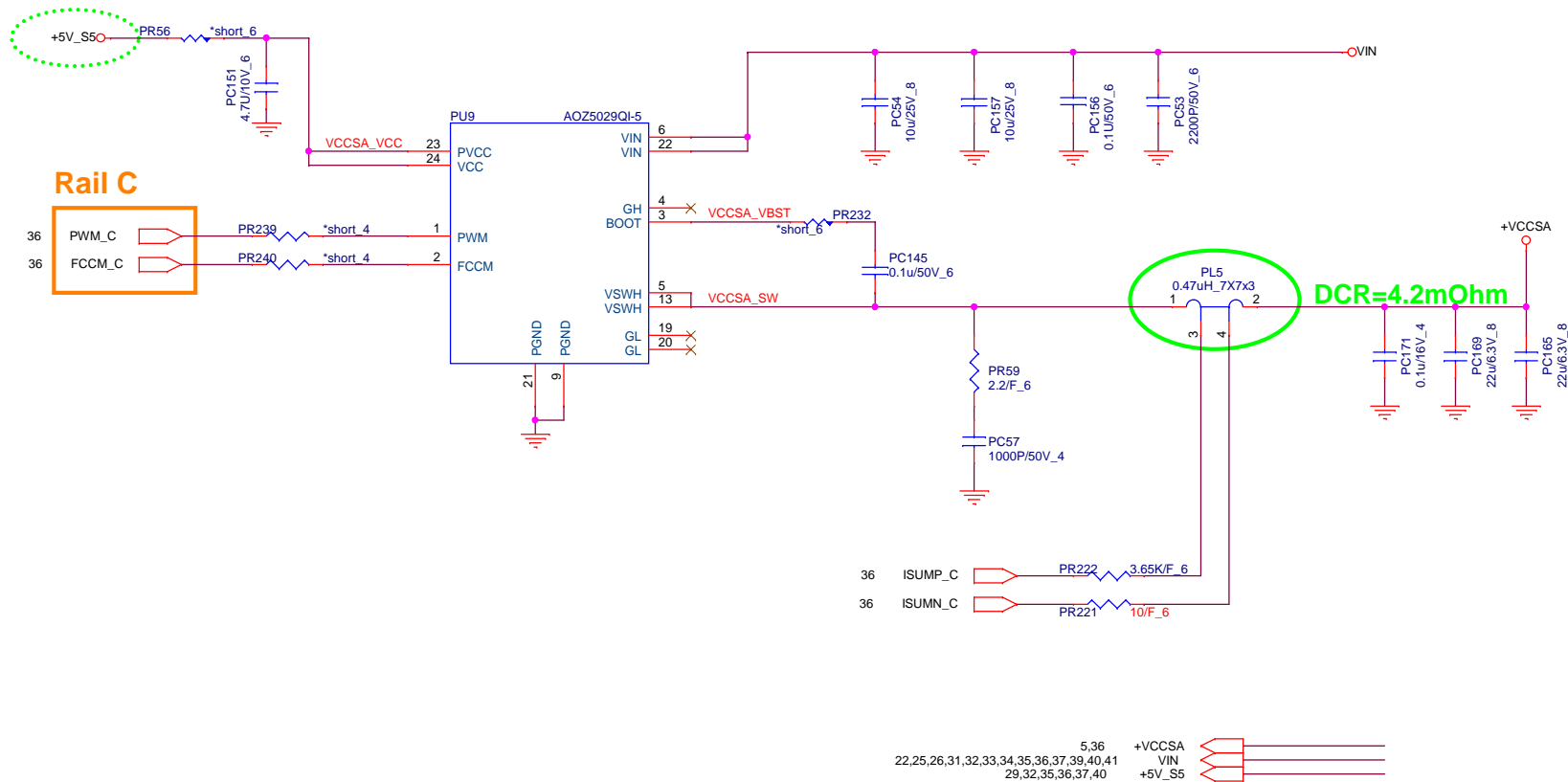
R_AC_LL : 2mV/A

VCCGT = 1 phase for U22, 不上件
VCCGT = 2 phase for U23e, 上件



5.36 +VCCORE
22,25,26,31,32,33,34,35,36,38,39,40,41 VIN
5.36 +VCCGT
29,32,35,36,38,40 +V, S5

VCCSA



VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

OCP : 6A

Fsw : 800KHz

VCCSA L/L :

R_DC_LL : 10.3mV/A

R_AC_LL : 10.3mV/A

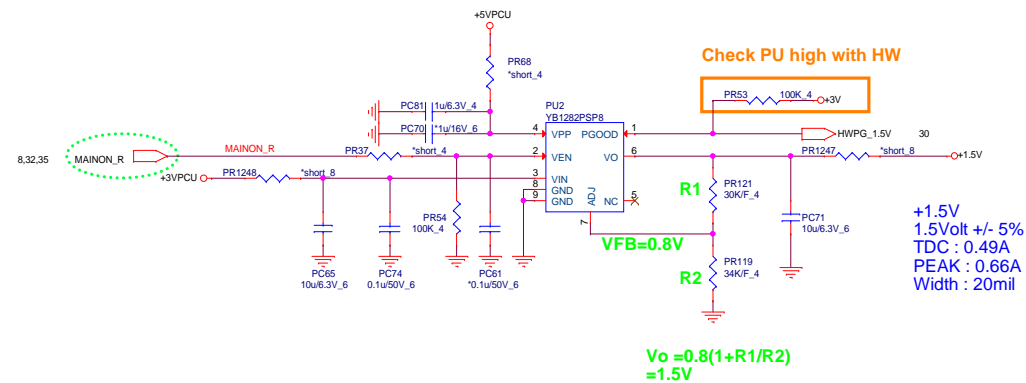
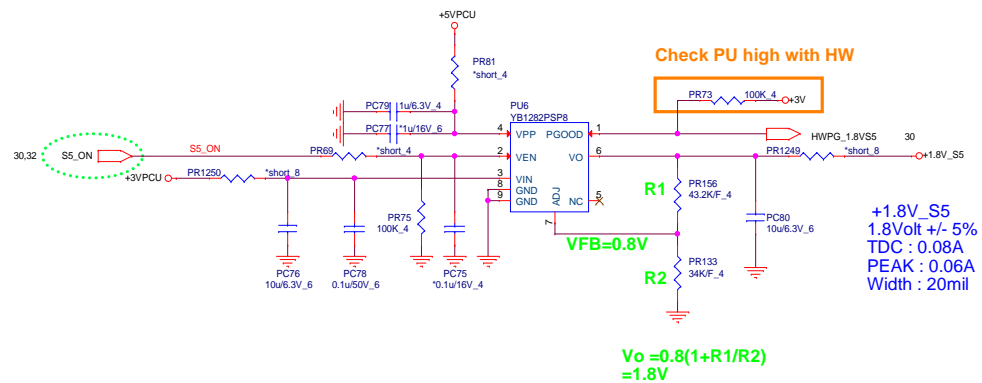


Quanta Computer Inc.

PROJECT : ZAA

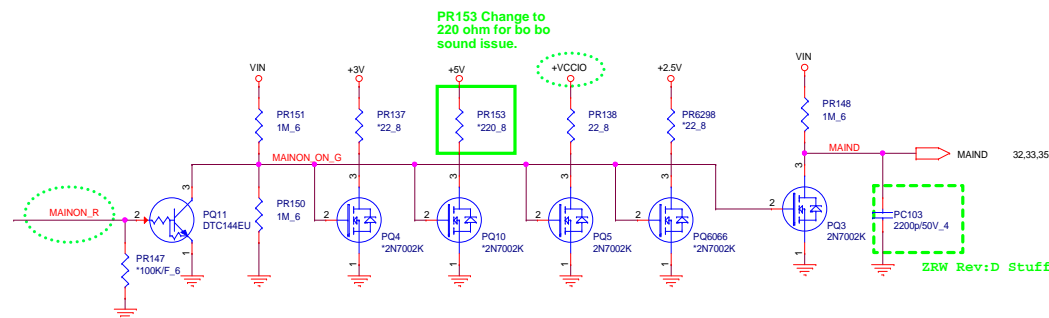
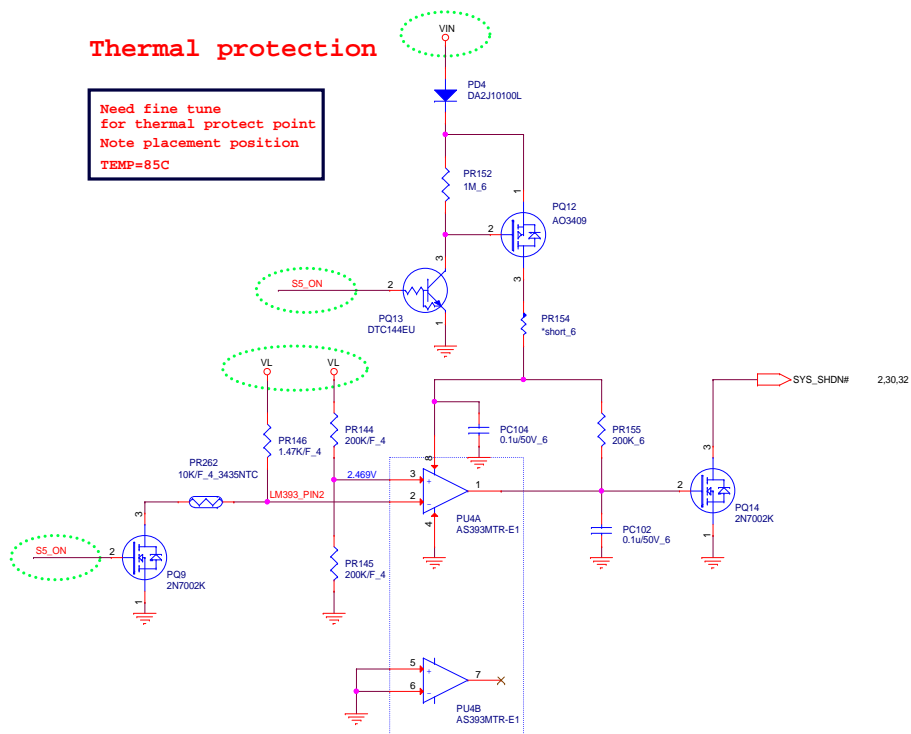
| Size | Document Number | Rev |
|------|------------------------------|-----|
| | VCCSA (ISL95808HRZ-T) | 1A |

Date: Monday, March 28, 2016 Sheet 38 of 48



Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C

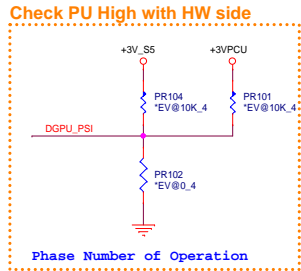


Quanta Computer Inc.
PROJECT : ZAA

| Size | Document Number | Rev |
|-------|-----------------------------|----------------|
| | +1.8V/+1.5V/Thermal Protect | 1A |
| Date: | Monday, March 28, 2016 | Sheet 39 of 48 |

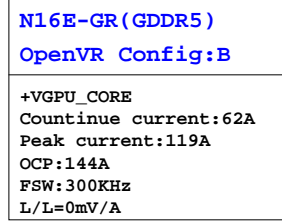
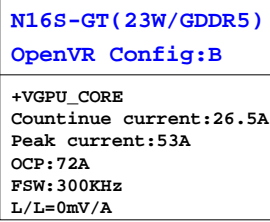
| | |
|--|---------------------------------------|
| 940 (23W): PR268 CS31242FB13 12.4K/F_4 | 950(40W): PR268 CS31002FB26 10K/F_4 |
| 940 (23W): PR270 CS26812FB13 6.81K/F_4 | 950(40W): PR270 CS25362FB15 5.36K/F_4 |
| 940 (23W): PQ41 Unstuff | 950(40W): PQ41 BAMB64140000 AON6414AL |
| 940 (23W): PQ42 Unstuff | 950(40W): PQ42 BAMB67520000 AON6752 |
| 940 (23W): PQ30 Unstuff | 950(40W): PQ30 BAMB64140000 AON6414AL |
| 940 (23W): PQ34 Unstuff | 950(40W): PQ34 BAMB67520000 AON6752 |


PR270 EV_SP@6.81K/F_4



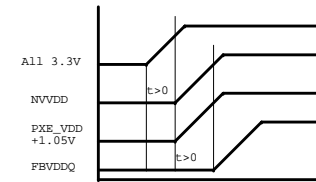
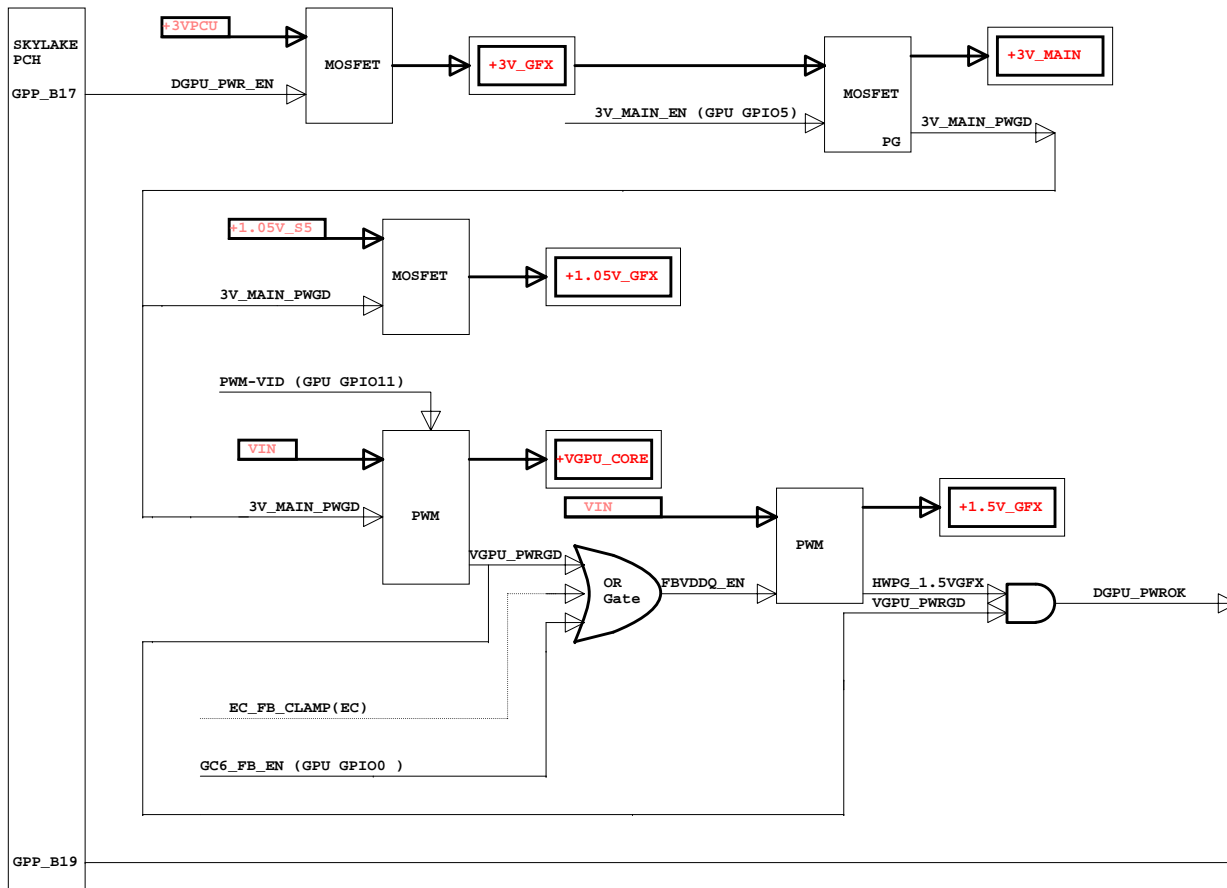
Standby Function

| Component Value | Config B |
|-----------------|----------|
| R1 | 20K |
| R2 | 20K |
| R3 | 2K |
| R4 | 18K |
| R5 | 0-ohm |
| C | 2.7nF |



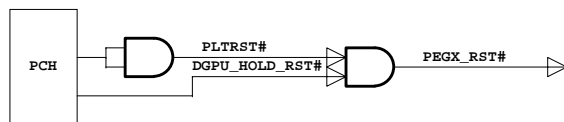
| | | |
|---|------------------------|----------------|
|  Quanta Computer Inc. PROJECT : ZAA | | Rev 1A |
| Size | Document Number | |
| +VGPU_CORE(UP1658RQKF) | | |
| Date: | Monday, March 28, 2016 | Sheet 40 of 48 |

VGA power up sequence

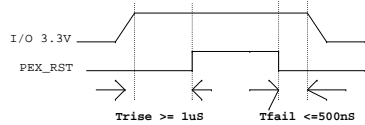


N15x Power on sequence
Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V includes all rails that are shared

VGA Reset

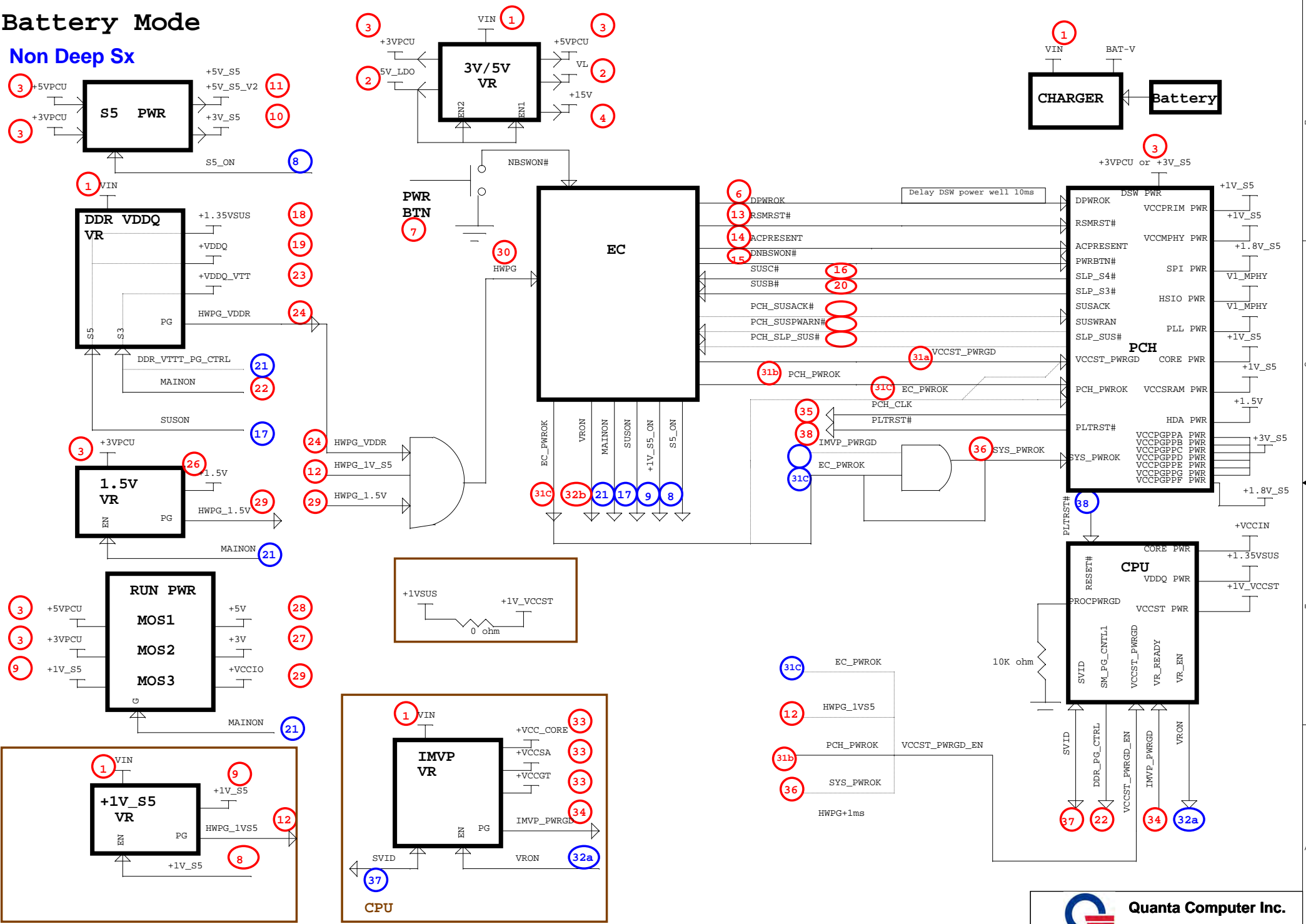


PEX_RST timing

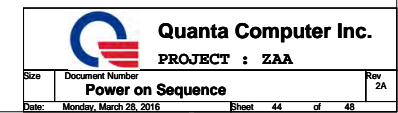


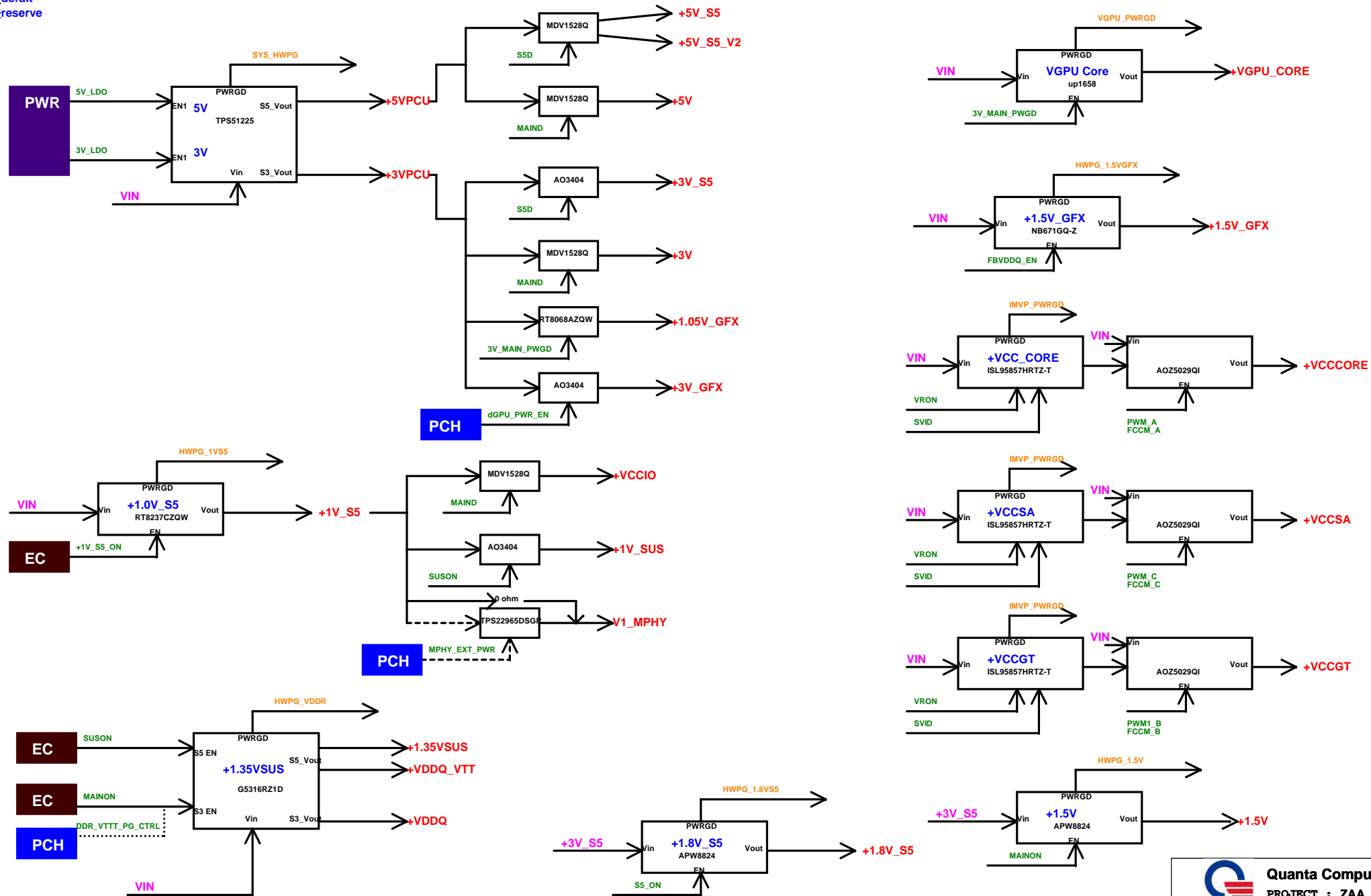
Battery Mode

Non Deep Sx

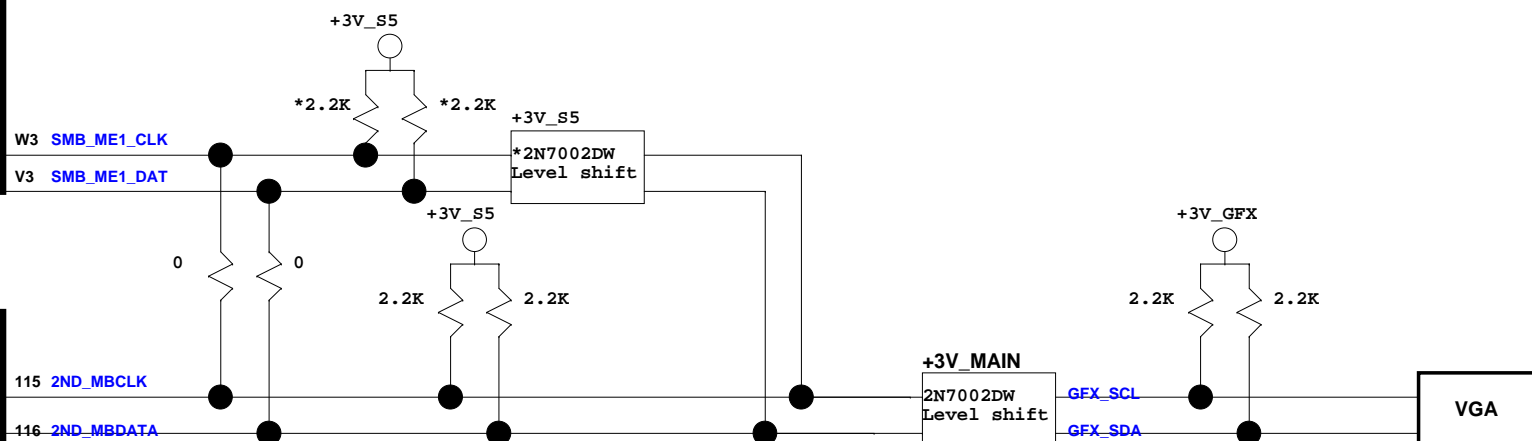
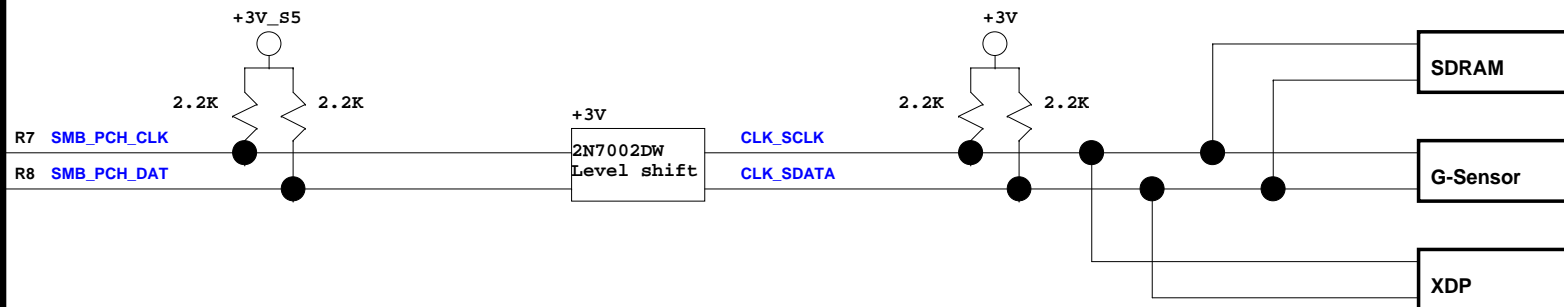


WWW.AliSaler.Com

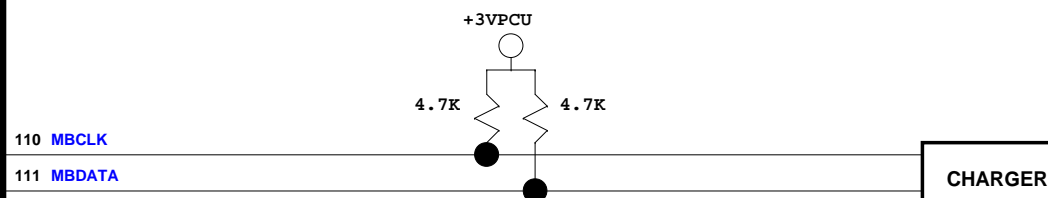




Skylake U



EC
IT8987CX



| Stage | Date | CHANGE LIST |
|-------|-------|--|
| A | 11/25 | 1. FIRST RELEASED |
| B | 12/11 | 1. Update DFDS15FR421, DFFC28FR026, DFFC08FR055, DFFC04FR127 to new footprint. 2. Remove IOAC@ part and change BOARD_ID3 to low (page 8.) 3. Change FAN connector CN8 to 3-pin, and add releven circuits. (page 28.) 4. For FAN function change, swap U45 pin-81 with pin-32. (page 30.) 5. Reserve G-sensor circuit. (page 28.) 6. Internal speaker signal short pad R419, R414, R406 & R404 change to 0603 0 ohm. (page 25.) 7. Remove extra hall-sensor circuit on 17". (page 22.) 8. Modify touchpad INT circuit by using R164. (page 4.) 9. Add EC52 TVS diode. (page 30.) 10. Dual DMIC LR pin change to pull-high. (page 25.) 11. Change R4314 & R4306 of value for KA/KB (page 17.) 12. Change R247 value from 0 to 2.2 Ohm (CS-2204FA00) (page 24.) 13. Change R251, R262, R269, R11265 footprint from 0603 to 0805 (page 24.) 14. Reserve R11282 for battery. (page 30.) 15. Change CN23 H=5.0 part number (page 28.) 16. R512 Change to 1% tolerance part number (page 6.) |
| | 12/14 | 1. Update CN6, CN8, CN18 part nmuber and foot print (page 25.) 2. Change U1006 part number to AL000103006 (page 26.) 3. Q6060 change to stuff (page 6.) 4. R628, R512, R630, R651, R4006 Change to 1% tolerance part number. |
| | 12/15 | 1. Update HOLE1, HOLE2 foot print to new Rev (page 27.) 2. Add HOLE25, PAD14 foot print (page 27.) 3. Change CN13, CN16 foot print to new Rev (page 23.) 4. Change cap CP to normal cap for keyboard (page 22.) 5. Reserve POA(FPD) circuit (page 26.) |
| | 12/20 | 1. Change PJ3 foot print to 50320-0040n-001-4p-1-smt for SMT issue (page 31.) 2. Change CPU 0201 Cap to 0402 besides C245, C196, C269, C285, C235 (page 5.) 3. Change SW4 foot print and part number for B-stage, and swap the pin (page 30.) 4. Modify some SPAD and HOLE (page 27.) 5. Change CN6 foot print to 50591-00401-001-4p-1 (page 28.) 6. Modify U22 Block GND pin 18-22 (page 29.) 7. Modify CN12, JDIM1, JDIM2, CN23, SW1, SW2 foot print to newer. |
| | 12/21 | 1. Change CN2021 foot print to ub31-dx07b024xjlar1000-24p (page 20.) 2. Change CN10 foot print to ngff-nase0-s6701-ts48-ke-smt (page 27.) 3. Add R11284 reserve DMIC power supply (page 25.) 4. Change C739 to 22pF and stuff for bit clocck issue (page 4.) |
| | 12/22 | 1. Change C1255, C1257, C1265, C1270, C1327, C4728 to 10uF cap for cost down (page 12, page 13.) |
| | 12/23 | 1. Modify R211, R152 to +3V_S5 for +3V leakage issue (page 8, page2.) 2. Modify R577 to reserved (NC), because no used (page 2.) 3. Add C4817, C4818, C4819, C4820 for EMI issue (page 20.) 4. Change CN2021 foot print to ub31-dx07b024xjlar1000-24p-smt (page 20.) 5. Change CN13, C16 foot print to ub3-yusb0021-p001a-9p-smt (page 29.) 6. Stuff R786, R568, R570, and unstuff U33, C628 (page 2, page 6.) 7. Swap PJ3 (page 31.) |
| | 12/24 | 1. Change CN4 foot print to sdcard-psdat4-11glbslnn4h4-11p (page 24.) 2. Change R11267, R11270 to short pad, and change R11268, R11271 form 33 ohm to 47 ohm (page 22.) 3. Unstuff C319, C333, C336, C716, C718 (page 22.) 4. Reserve R11285, R11286 pull up to +3V, and R11287 pull down to GND for CRT issue (page 21.) 5. Stuff R11286 for CRT issue (page 21.) 6. Remove all type-C re-driver short resistor and capacitor (page 20.) |
| | 12/25 | 1. Change HOLE16 foot print to H-TC217BC197D126P2 (page 24.) |
| | 12/29 | 1. Modify the power solution between GT2 and GT3e, see the table (page 36.) 2. Change the power value, PC10 to 1uF CH5101K9B01 (page 36.) 3. Change the power value, PC20 to 0.022uF CH3224K1B01 (page 36.) 4. Change the power value, PC28 to 560pF CH1566K1B09 (page 36.) 5. Change the power value, PC39 to 0.015uF CH3154K1B00 (page 36.) 6. Change the power value, PR220 to 475 ohm CS14752FB11 (page 36.) 7. Modify BOARD_ID7. GPU GT, KB, GTR PU 10k ohm, KA PD 10k. (page 8.) 8. Change the RTC clock crystal Y2 part number to BG3327680C6 (page 6.) 9. Change Q115, Q129 part number to BAM70020076 (page 19.) 10. Modify R11283 to +3V fixed the SSD issue (page 27.) 11. Change the HOLE16 NUT part number to MBZAA002010 (page 27.) |
| B2 | 1/7 | 1. Remove R11274 and mount R11277 for change equalizer setting from 6dB to 4dB (page. 23) 2. Change 15" and 17" keyboard part number to DFFC28FR030 (page 28.) |
| | 1/18 | 1. Update the System Block Diagram (page 1.) 2. Update the part number option same as B-SMT BOM. |
| | 1/19 | 1. Power team remove JUMP and change 0 ohm to shortpad (page 31-41.) 2. Modify some description, value and part number have blank. |
| | 1/20 | 1. Change C144,C150,C190,C199,C248,C645,C650,C659,C666,C690,C696,C697,C702 to 22uF, part number : CH6221M9A00 (page 5.) 2. Change C171,C178,C203,C219,C224,C226,C233,C236,C243,C251,C255,C272,C273,C282,C289,C691,C692,C693,C694,C703,C704,C705,C706,C707,C202,C210 to 10uF, part number : CH6101M9905 (page 5.) |
| | 1/21 | 1. Change D2,D3,D4,D5,D4013,D4014,EC51,EC52 main source part number from BC040201Z00 to BC005725Z00. |

| | | | | | | | | | | | | | | | |
|--|--|----------------------|--|----------------|--|-----------------|--|-----|--|--------------|--|----|--|-----------|--|
|  | | Quanta Computer Inc. | | DOC NO. | | PROJECT MODEL : | | ZWA | | APPROVED BY: | | | | DATE: | |
| PROJECT : ZAA | | | | | | | | | | | | | | | |
| File | | Document Number | | Rev | | PART NUMBER: | | | | DRAWING BY: | | | | REVISION: | |
| Change list | | | | | | | | | | | | | | | |
| Date | | Version | | March 28, 2016 | | Rev | | 57 | | of | | 65 | | | |

| Stage | Date | CHANGE LIST |
|-------|------|---|
| C | 1/22 | 1. Reserve R11288, R11289, R11290, R11291 0ohm for POA NC function (page 26.) 2. Change Q115, Q129 main source to BAM70020002 3. Change Q5, Q4201 main source to BA039040020. 4. Change D7, D4000 main source to BCBAT54CZ01. 5. Change Q3, Q32, Q4301 main source to BAM70020047. |
| | 1/26 | 1. Change CN5 part number to DFHS40FS036 (page 22.) 2. Change CN4 part number to DFHS11FR170 (page 4.) 3. Modify POA circuit for C-stage test (page 26.) |
| | 1/27 | 1. Change the TPS25810RVC pu-high power from +5V_S5_V2 to +3V_S5 (page 20.) 2. Reserve R11193 for Type-C detec issue (page 20.) 3. Change 0 Ohm to short pad R11,R14,R15,R28,R66,R67,R11129,R102,R194,R224,R229,R235,R790,R791,R792,R11111,R11112,R11113,R11140,R112,R135,R179,R180,R182,R185,R187,R188,R192,R193,R198,R240,R252,R11131,R164,R246,R339,R350,R11185,R11186,R550,R657,R718,R721,R782,R11153,R11283,R795,R796,R797,R816,R817,R818,R819,R820,R821,R11196,R11199,R11202,R11207,R11279,R11280,R11281,R948,R951,R956,R958,R959,R960,R11061,R11062,R11110,R11133,R11134,R11136,R11137,R11138,R11139,R11141,R11253,R11254,R11255,R11256,R11267,R11270,R4328,R4335,R2855,R2870,R318,R221,R403,R405,R742,R743,R725,R745,L19,R2872. 4. Add TYPE@ part at Type-C power function (page 32.) 5. Add BL@ part at keyboard back-light (page 28.) 6. Reserve 15" 17" Dual DMIC circuit part (page 25.) 7. Reserve C4821 for NAC function (page 24.) |
| | 1/28 | 1. Add EV@ part at HOLE8, HOLE9 (page 27.) |
| | 1/29 | 1. Stuff PR233, PR234 for GT3e power function (page 37.) 2. Add D22@, D10@ part at CPU power side (page 5.) 3. Change PR209, PR210 from short pad to 10 ohm (page 31.) |
| | 2/2 | 1. Modify POA circuit for C-stage test (page 26.) 2. Remove HOLE25 because not used (page 25.) 3. Change HOLE13, HOLE14, HOLE15 foot print to H-C256D161P2 (page 25.) |
| | 2/3 | 1. Modify POA circuit for C-stage test (page 26.) 2. Change PC115 from CH5104K9906 to CH41006K911 for FAE suggest (page31.) 3. Stuff PC138 for FAE suggest (page 37.) |
| | 2/4 | 1. Update C-test BOM. |
| | 2/16 | 1. Change PR6121 from CS31002FB26 to CS29312FB13 (page 32.) 2. Add C376 distinguish ZAA/ZAAA 15" serial and ZYJ/ZYI 17" serial (page 25.) 3. Change LED current limiting resistor blue and orange to 47 ohm and 124 ohm (page 28.) |
| | 2/17 | 1. Change PU6010 from AL006575002 to AL051225003 for 3/5V IC noise issue (page 32.) |
| RAMP | 2/22 | 1. Stuff PC6229, PC6212 for 3/5 voltage IC noise and charging issue (page 32, 37.) 2. Change PR183, PR184, PR209, PR210 to shortpad for 3/5 voltage IC noise and charging issue (page 31.) 3. Modify RP1 circuit (page 28.) |
| | 3/3 | 1. Unstuff R694, R699 (page 27.) 2. Change 0 Ohm to shortpad R3, R4 R365, R640, R653, R659, R668, R11191, R11192, R16, R212, R404, R406, R414, R419, R752, R789, R237, R672. 3. Remove RP2, RP3, RP4, RP5, L69 for SMT colay issue. (page 20.) |
| | 3/9 | 1. Change 0 Ohm to shortpad R11284, R2870, R2872, R11298, PR6296, R4329, R4336, PR112. 2. Change PR201, PR202 and PR211 to 1.5k, 97.6k and 267 ohm for GT2 and GT3 (page 36.) 3. Add PC6232, PC6233 at 3/5 V Vin (page 32.) 4. Change PL6013 from 1uH_7X7X3 to 2.2uH_7X7X3 (page 32.) |
| | 3/10 | 1. Change C714 and C724 value from 10p to 1000p for projector issue (page 22.) 2. Remove SW2 for RAMP-stage (page 30.) 3. Change PU10, PU11, PU20 footprint to son14-3x2-4-15p-smt (page 32.) |
| | 3/15 | 1. Change RTC crystal circuit C351 and C362 value from 6.8p to 15p for EA issue (page 22.) 2. Modify GPU power solution for cost down (page 40.) |
| | 3/25 | 1. Change R237 shortpad to 0 ohm for next PCB rev. F (page 27.) 2. Reserve POA function (page 26.) |

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|--|----------------------|---------|--|-----------------|-----|--------------|-----------|
|  | Quanta Computer Inc. | | | | | | |
| PROJECT : | ZAA | DOC NO. | | PROJECT MODEL : | ZWA | APPROVED BY: | |
| DESIGN : | | | | PART NUMBER | | DRAWING BY: | |
| DATE : | | | | | | | REVISION: |